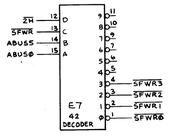
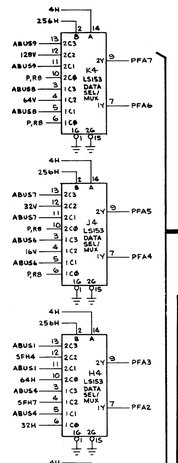
VIDEO GENERATOR

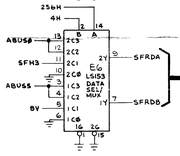
The address decoder outputs the scrollfield write enable signal $\overline{SFWR}$, and the microprocessor selects the appropriate RAM pair with address lines ABU50 and ABU55.



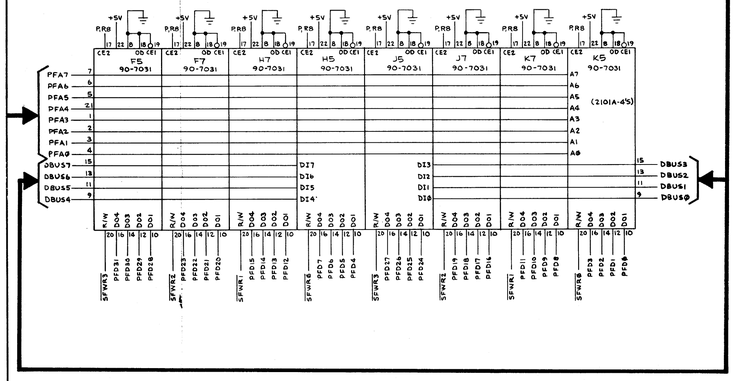
Data Selectors F4, H4, J4 and K4 select the addressing mode for the Video Generator RAM. When 4H is high, the MPU addresses the RAM, via ABUS 0-9. When 4H is low, the Video Generator RAM is addressed by either the scrollfield horizontal address (SFH 3-7) or by the sync chain (8H-64H and 16V-128V). 256H determines which of these two addresses the RAM when 4H is low. When 256H is low sync is selected. When 256H is high, scrollfield is selected.



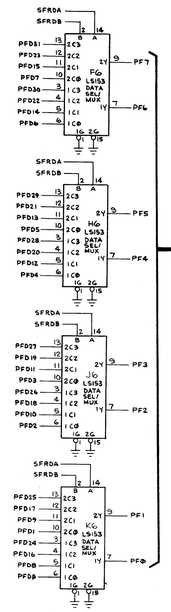
Multiplexer E6 selects the output of the RAM.



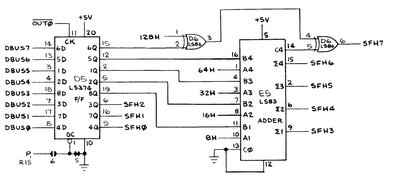
VIDEO GENERATOR RAM



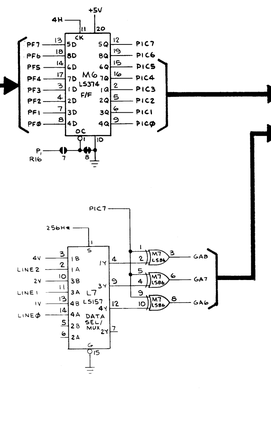
When the RAM is written to by the microprocessor, $\overline{SFWR}$ is low and a RAM pair is written to by the selection of ABUS0 and ABUS5. Data is written into the RAM through data bus DBUS0 thru DBUS7. Data is read out of the RAM on data lines PFD0 thru PFD31.



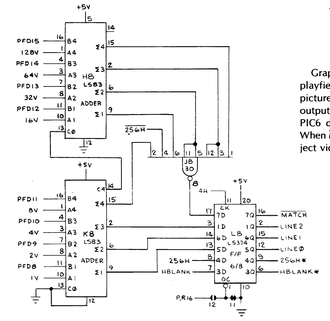
The latched data output of D5 is compared with horizontal sync 8H thru 64H, to enable the playfield to scroll (shift) in steps of 8H. SFH0 thru SFH2 selects the scrollfield output from multiplexer C8 in steps of 1H.



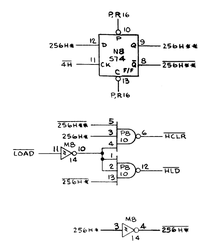
The microprocessor reads the latched playfield and motion objects data bytes on data lines D0 thru D7.



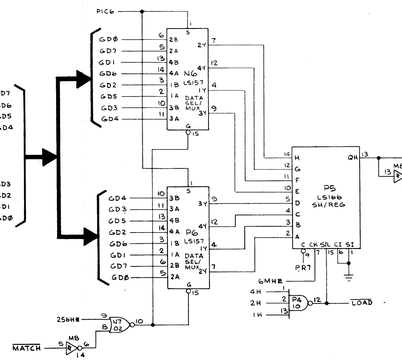
Graphics PROMs M5 and N5 contain the graphics data for both the playfield and motion objects. Address inputs PIC0 thru PIC5 select the picture. Inputs GA6 thru GA8 select the actual line of the picture to be output. PIC7 determines whether or not the picture is reflected vertically. PIC6 determines whether or not the picture is reflected horizontally. When $\overline{MATCH}$ is low, the multiplexers are enabled for writing motion object video data into motion object RAM B6.



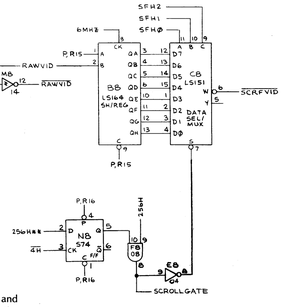
Adders H8 and K8 compare the vertical line presently being scanned with RAM data PFD8 thru PFD15, which define the vertical location of the motion object. When the inputs are equal, $\overline{MATCH}$ is latched low, permitting the motion object data to be output from the graphics PROM. LINE0 thru LINE2 count up for the eight scan lines of the motion object picture.

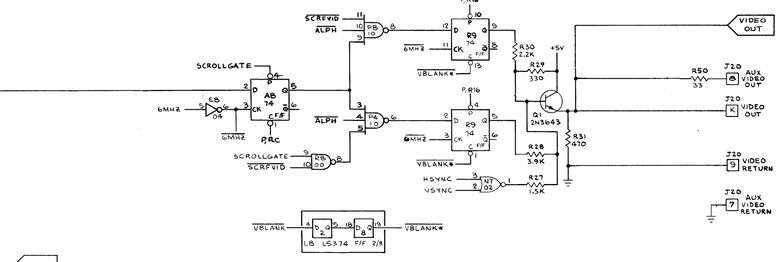


The alphanumerics, playfield, motion objects video and vertical and horizontal sync signals are all summed at the video summer. The $\overline{VBLANK}$ signal ensures that there is no video during the vertical blanking period.



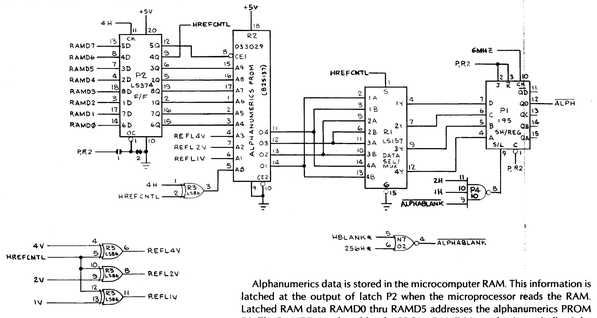
The SCROLLGATE signal ensures that the playfield and motion object video is only output during the portion of the screen scanned, when 256H is high, conditioned by 256H**.



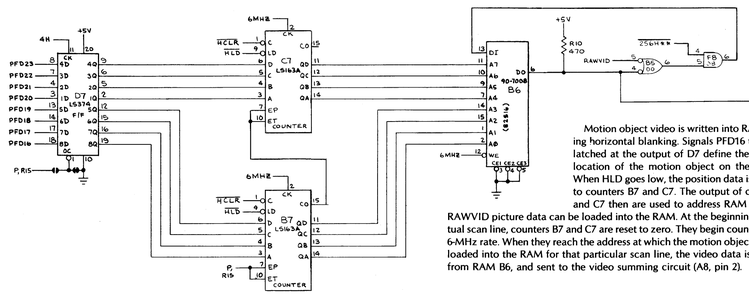


denotes a test point

ALPHANUMERICS GENERATOR



Alphanumerics data is stored in the microcomputer RAM. This information is latched at the output of latch P2 when the microprocessor reads the RAM. Latched RAM data RAMD0 thru RAMD5 addresses the alphanumerics PROM R2. The RAMD7 signal enables the PROM. RAMD6 is used to invert (reflect) the data output of the PROM both horizontally and vertically at the output of multiplexer R1. Therefore, the same data output is used at both ends of the monitor. The ALPHABLANK signal ensures that the alphanumerics appear only at each end of the horizontal scan line.



Motion object video is written into RAM B6 during horizontal blanking. Signals PFD16 thru PFD23 latched at the output of D7 define the horizontal location of the motion object on the scan line. When HLD goes low, the position data is loaded into counters B7 and C7. The output of counters B7 and C7 then are used to address RAM B6, so that RAWVID picture data can be loaded into the RAM. At the beginning of the actual scan line, counters B7 and C7 are reset to zero. They begin counting up at a 6-MHz rate. When they reach the address at which the motion object video was loaded into the RAM for that particular scan line, the video data is outputted from RAM B6, and sent to the video summing circuit (A8, pin 2).

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4-PLAYER FOOTBALL VIDEO GENERATOR AND ALPHANUMERICS GENERATOR
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