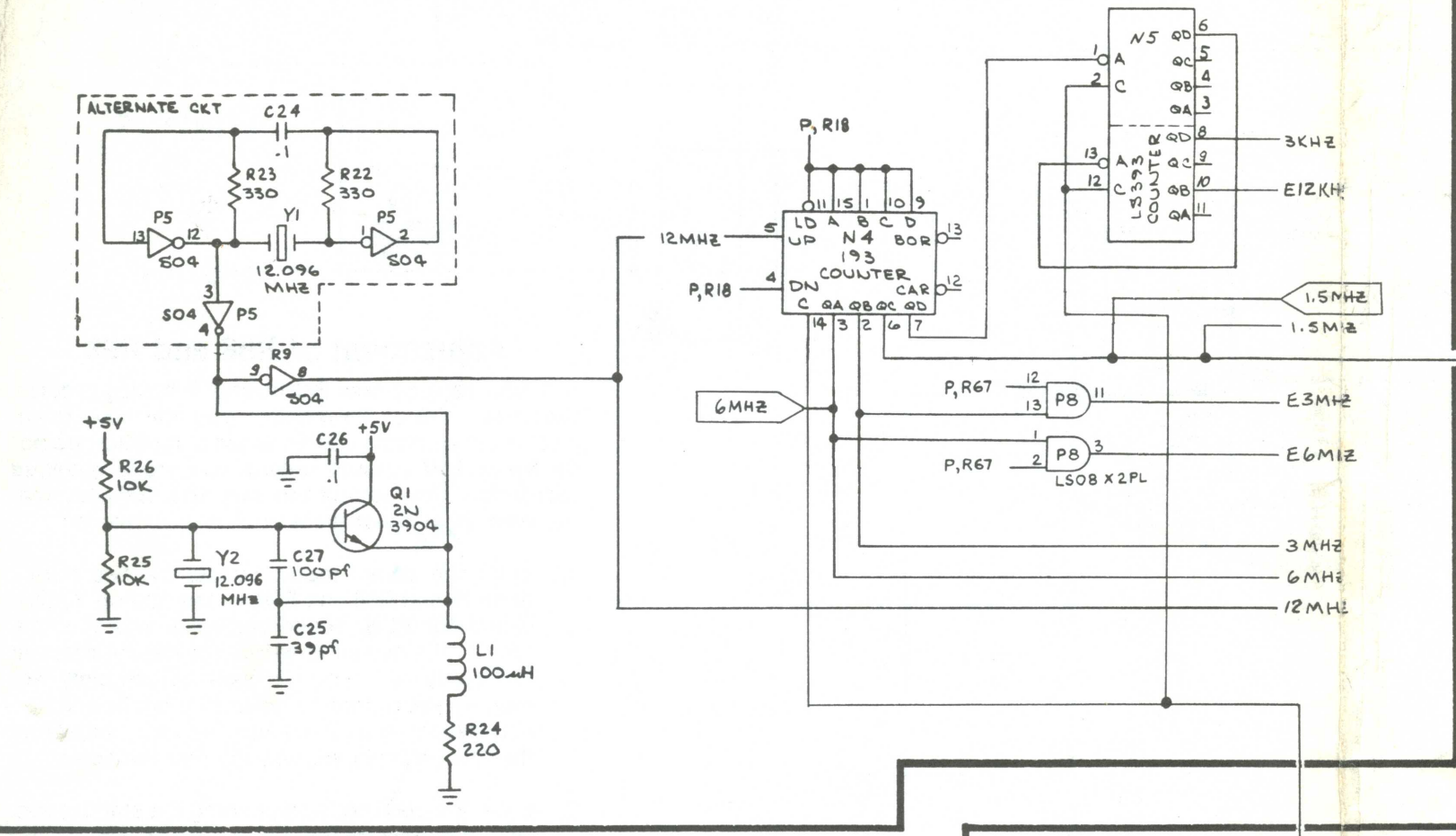
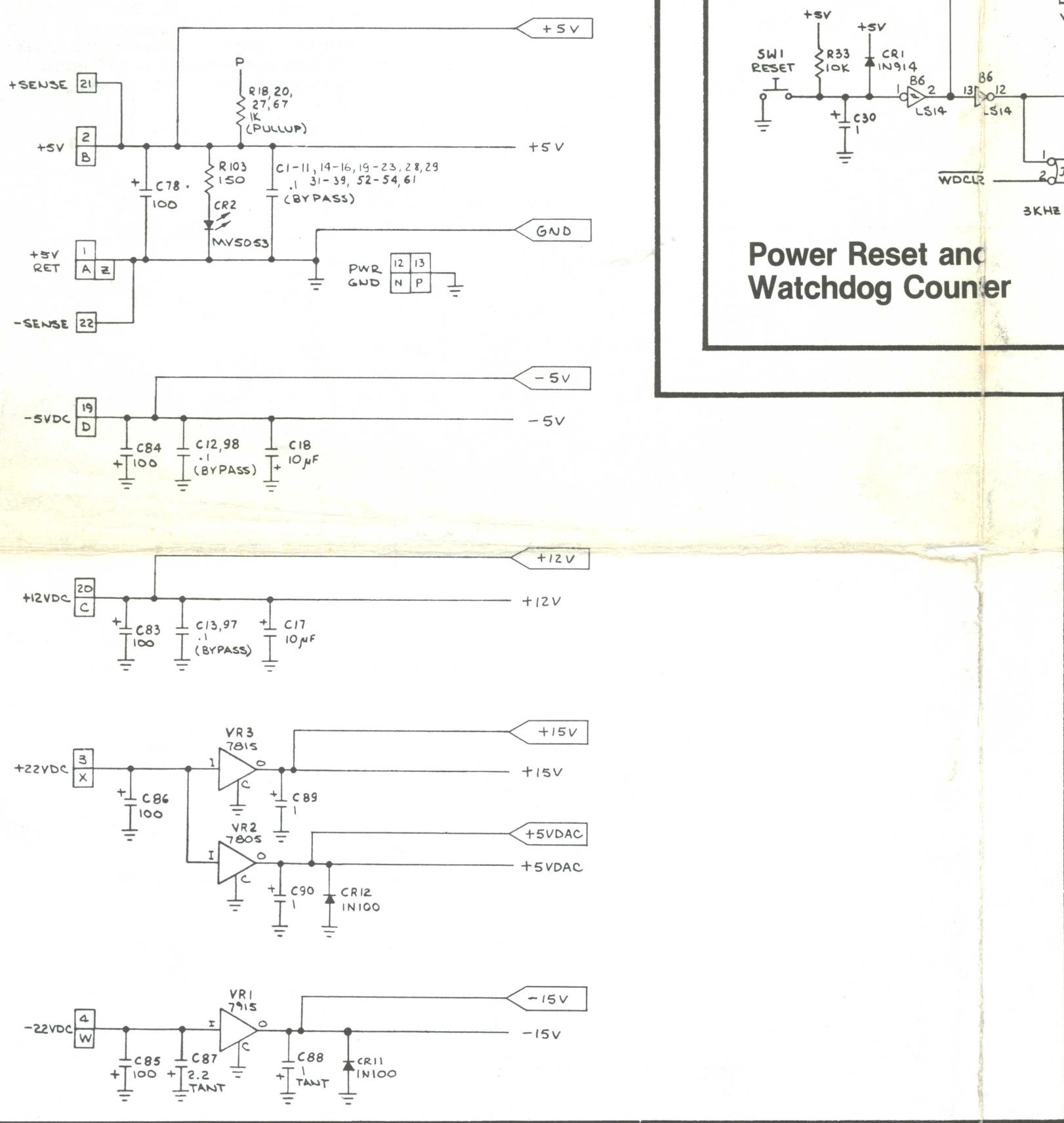


Clock



Power Input

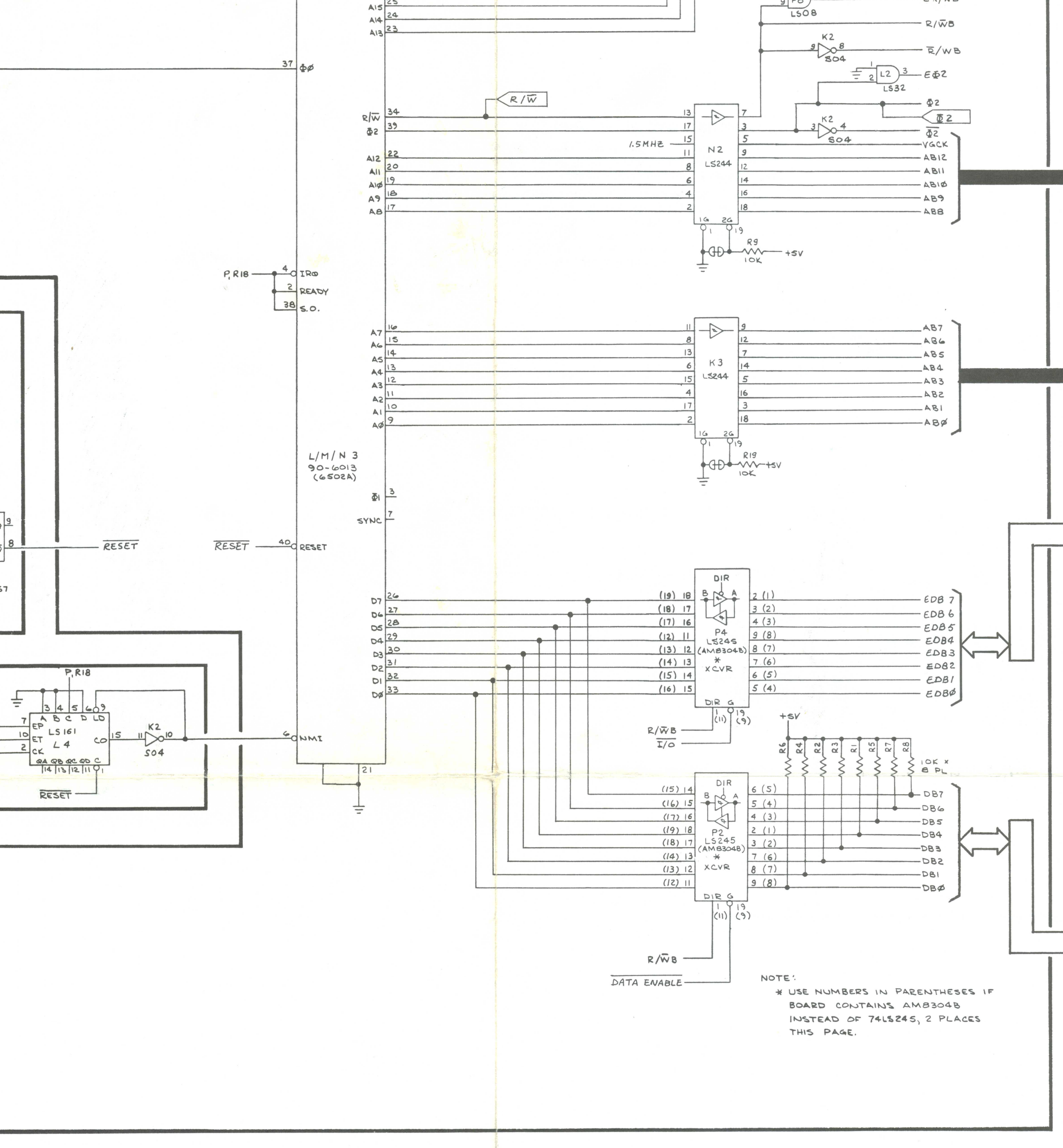


Sheet 2, Side A
BATTLEZONE™
 Game Microprocessor
 Game Address Decoding Circuitry
 Analog Vector-Generator PCB Power Input
 Clock
 NMI Counter
 Power Reset and Watchdog Counter
 Game Program Memory
 Game RAM
 Game Memory Map
 Section of 035742-01 & -02 B

NOTICE TO ALL PERSONS RECEIVING THIS DRAWING
 CONFIDENTIAL. Reproduction forbidden without the
 specific written permission of Atari, Inc., Sunnyvale, CA.
 This drawing is only conditionally issued, and neither
 receipt nor possession in itself conveys or transfers any
 right in, or license to use, the subject matter of the draw-
 ing or any design or technical information shown thereon,
 nor any right to reproduce this drawing or any part
 thereof. Except for manufacture by vendors of Atari, Inc.,
 and for manufacture under the corporation's written
 license, no right to reproduce this drawing is granted or
 the subject matter thereof unless by written agreement
 with or written permission from the corporation.

TEST CONNECTOR - FOR ATARI MANUFACTURING ONLY

Microprocessor

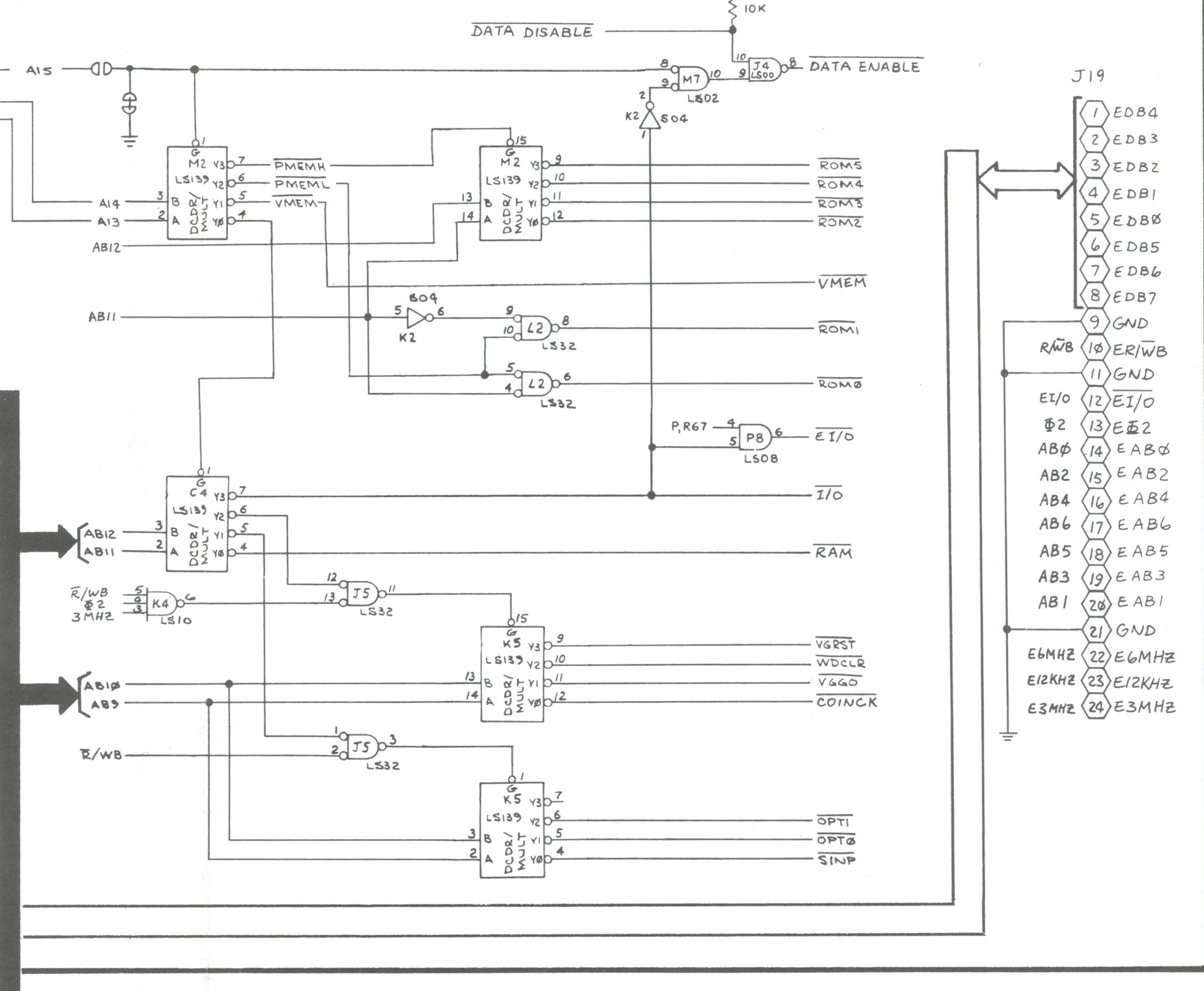


MEMORY MAP

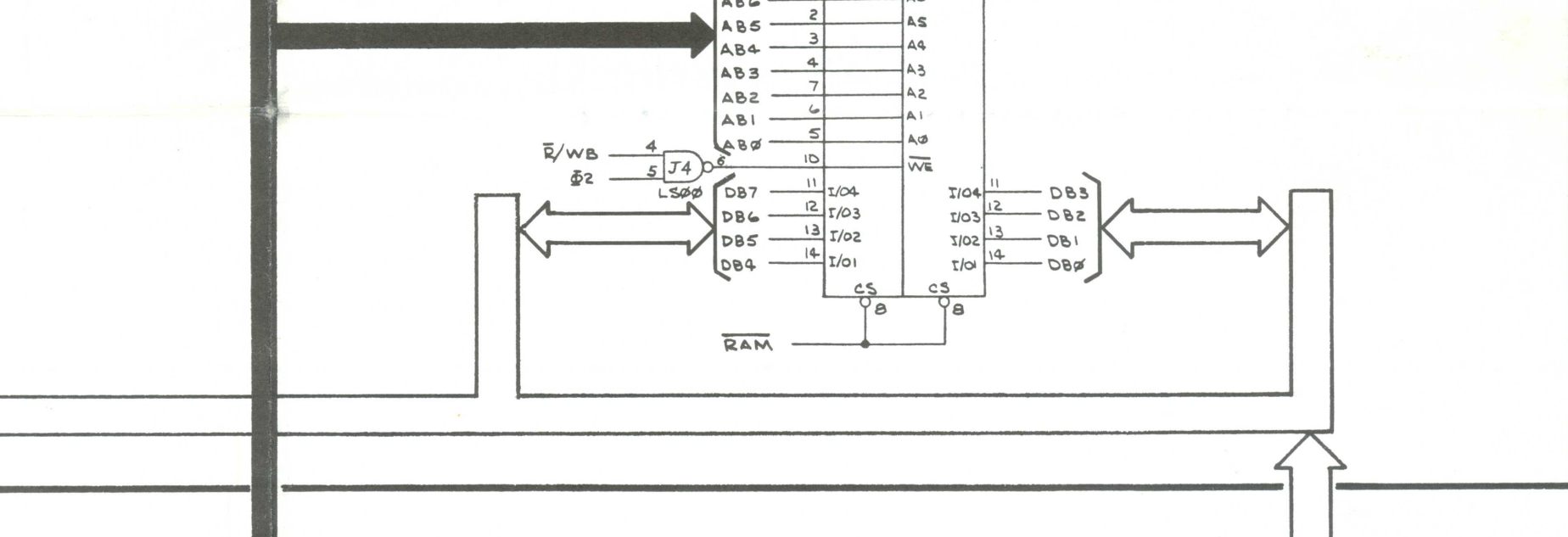
HEXADEDECIMAL	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF	0	0	0	0	0	0	0	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	PROGRAM RAM (1K)	
0800	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	RIGHT COIN SWITCH	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	CENTER COIN SWITCH	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	LEFT COIN SWITCH	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	SLAM SWITCH	
0A00	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	SELF TEST SWITCH	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	CENTER COIN SWITCH	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	DIAG STEP SWITCH	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	HALT	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	3 KHZ	
	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	OPTION SWITCH INPUTS	
0C00	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	OPTION SWITCH INPUTS	
1000	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	OPTION SWITCH INPUTS	
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	COIN COUNTER RIGHT	
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	COIN COUNTER CENTER	
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	COIN COUNTER LEFT	
	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	VIDEO INVERT X	
1200	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	VIDEO INVERT Y	
1400	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	VECTOR GENERATOR GO	
1600	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	WATCHDOG CLEAR	
1800-187F	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	W	D	D	D	D	D	D	D	VECTOR GENERATOR RESET	
	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R	D	D	D	D	D	D	D	AUXILIARY PCB ENABLE	
2000-27FF	0	1	0	0	0	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	VECTOR RAM (2K)	
2800-2FFF	0	1	0	0	1	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	VECTOR RAM/VECTOR ROM (2K)	
3000-3FFF	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	VECTOR ROM (4K)	
5000-5FFF	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	PROGRAM ROM (4K)	
8000-7FFF	1	1	A	A	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	PROGRAM ROM (8K)	

NOTE
 □ Indicates Edge Connector
 ○ Indicates Interconnect Connector
 ◀ Indicates Test Point

Address Decoder



RAM Memory



Program Memory

