Table of Contents

NOTE

This staple temporarily holds the schematic package together. Remove the staple before using the schematics.

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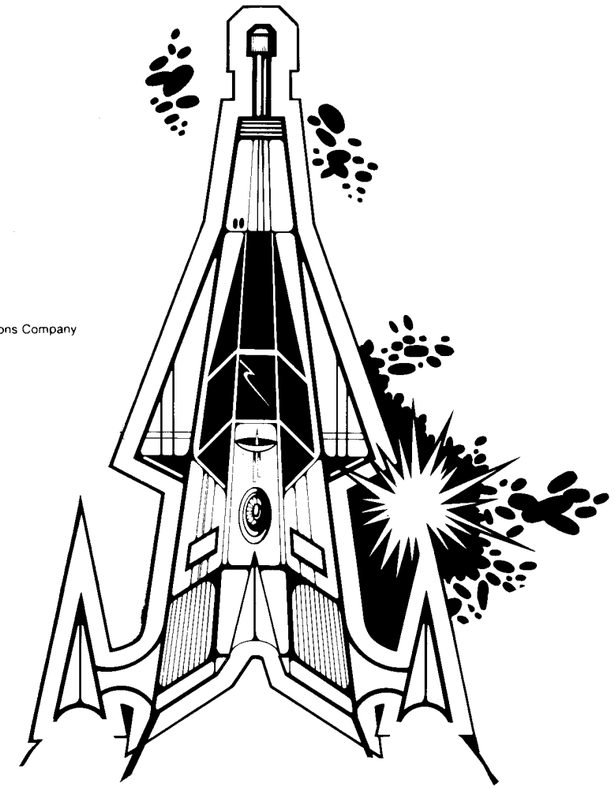
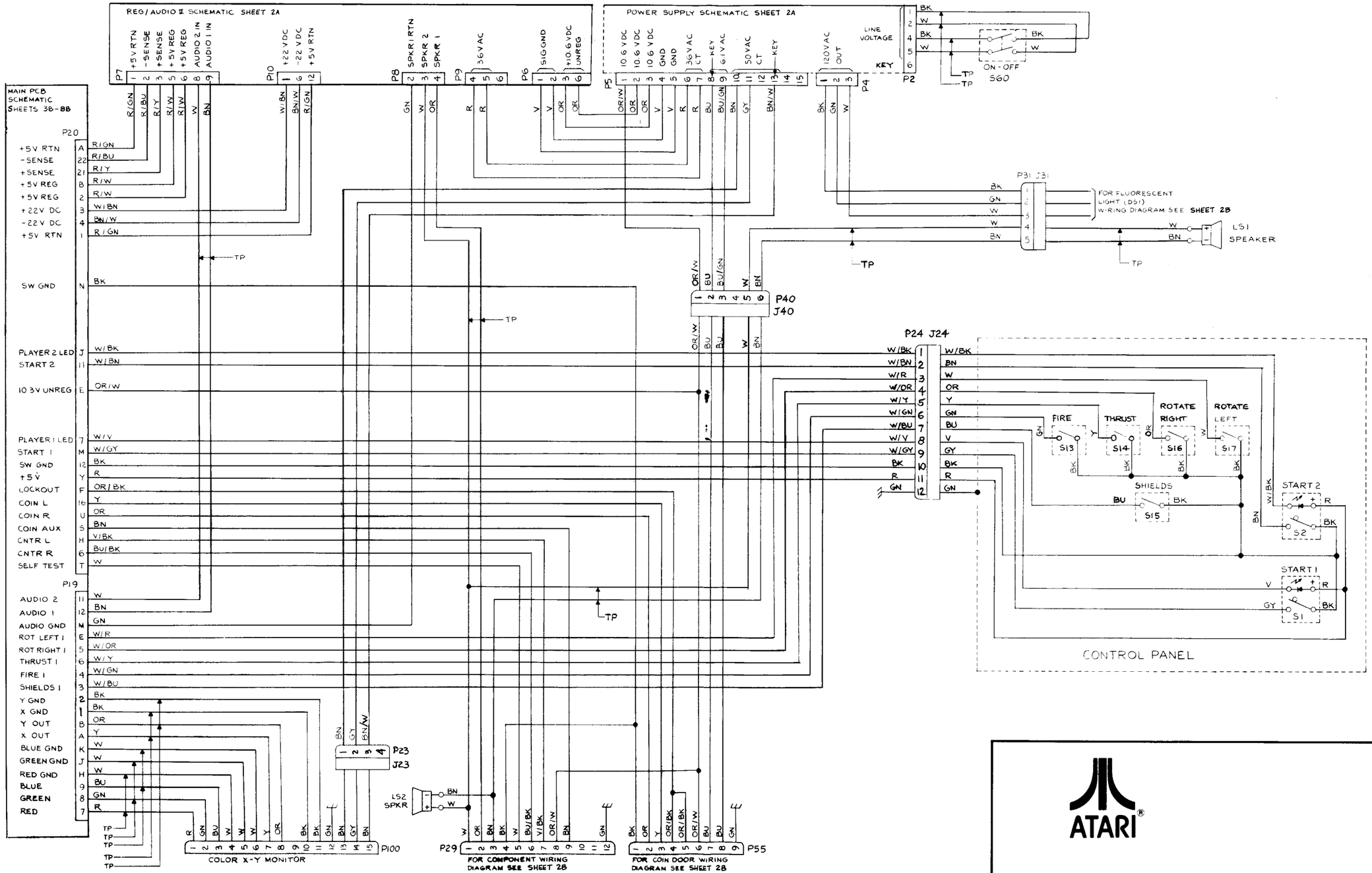


Schematic Package Supplement to GRAVITAR™

Operation, Maintenance and Service Manual

7L

SP-206 Sheet 1A
1st printing



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Gravitar Main Wiring Diagram

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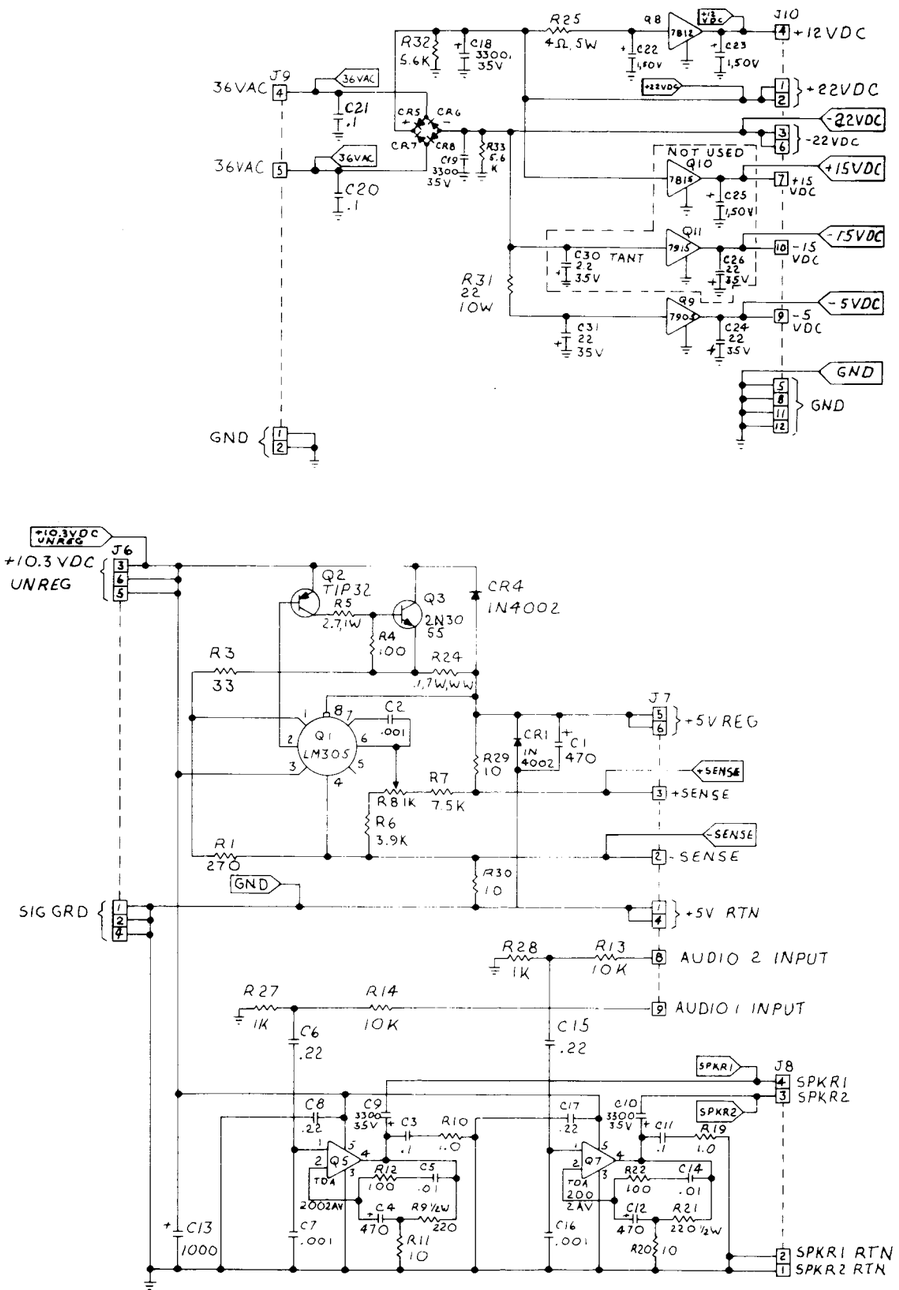
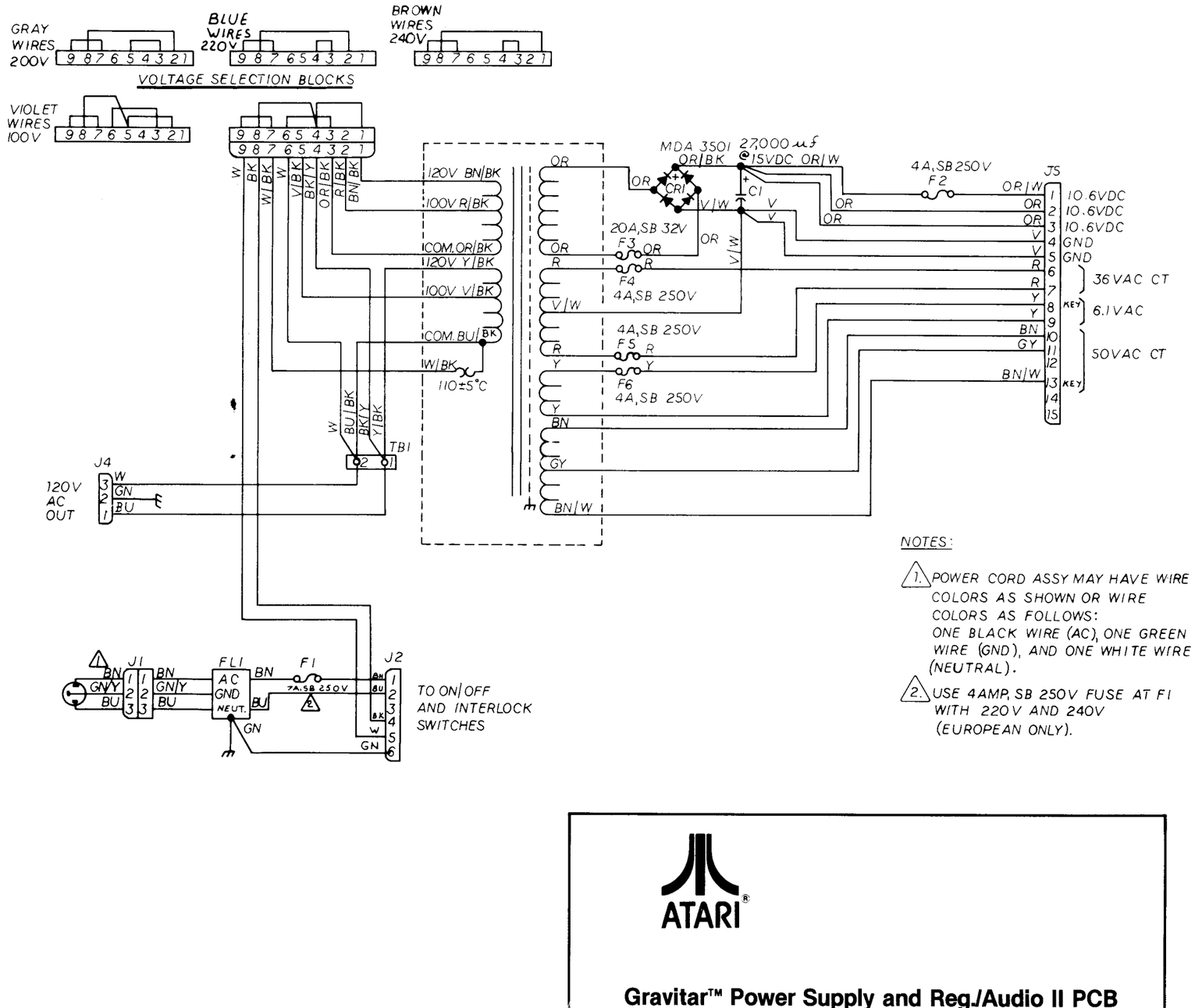
Regulator/Audio II PCB Schematic Diagram



COLOR X-Y POWER SUPPLY DIAGRAM



NOTES:

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND), AND ONE WHITE WIRE (NEUTRAL).
2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V AND 240V (EUROPEAN ONLY).

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Gravitar™ Power Supply and Reg./Audio II PCB

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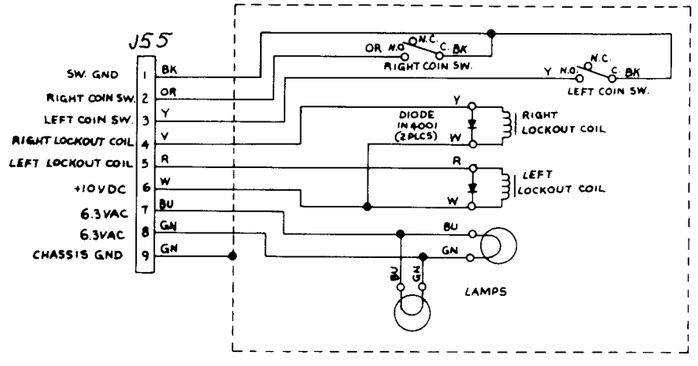
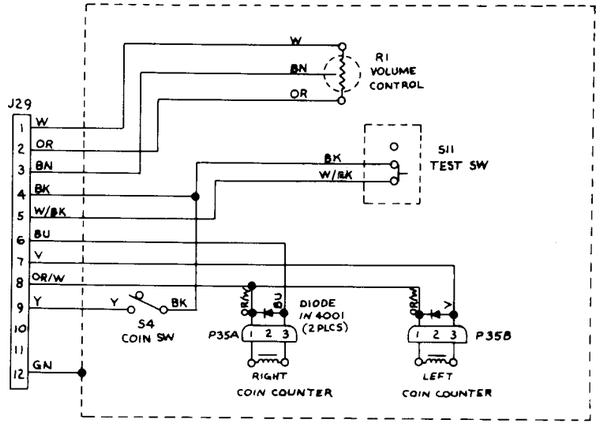
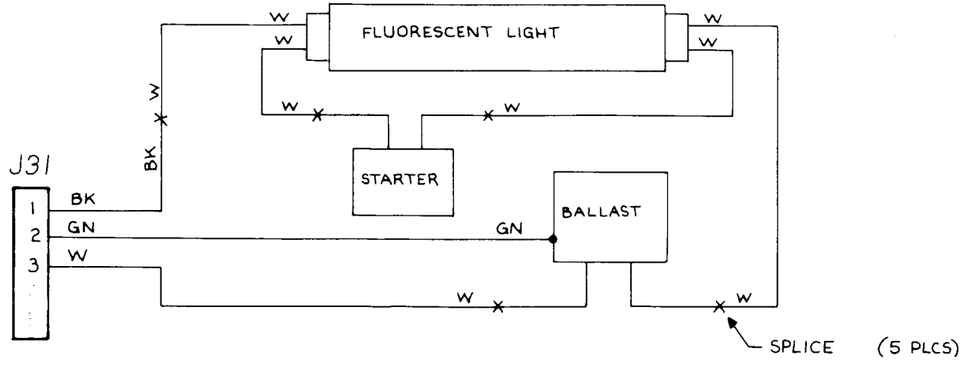
Coin Door Wiring Diagram



Utility Panel Wiring Diagram



Fluorescent Light and Speaker Wiring Diagram



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Gravitar™ Game Wiring Interfaces

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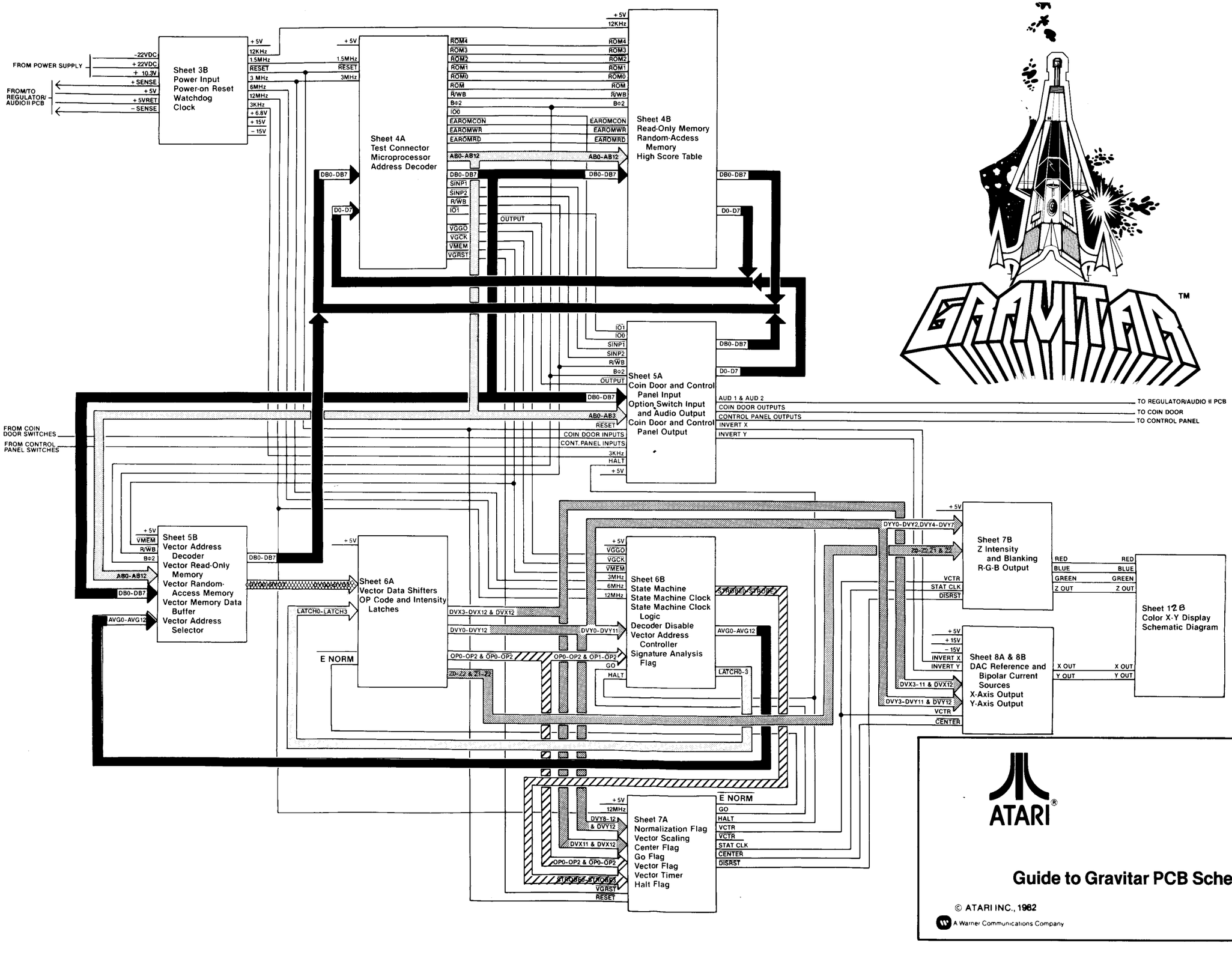
FROM POWER SUPPLY
-22VDC
+22VDC
+ 10.3V
+ SENSE
FROM/TO REGULATOR/ AUDIO II PCB
+ 5V
+ 5VRET
- SENSE
Sheet 3B
Power Input
Power-on Reset
Watchdog
Clock
+ 5V
12KHz
1.5MHz
RESET
3 MHz
6MHz
12MHz
3KHz
+ 6.8V
+ 15V
- 15V
Sheet 4A
Test Connector
Microprocessor
Address Decoder
ROM4
ROM3
ROM2
ROM1
ROM0
ROM
R/WB
B∅2
IO0
EAROMCON
EAROMWR
EAROMRD
AB0-AB12
DB0-DB7
SINP1
SINP2
IO1
OUTPUT
VGGO
VGCK
VMEM
VGRST
D0-D7
Sheet 4B
Read-Only Memory
Random-Acdess
Memory
High Score Table
Sheet 5A
Coin Door and Control
Panel Input
Option Switch Input
and Audio Output
Coin Door and Control
Panel Output
AB0-AB3
RESET
COIN DOOR INPUTS
CONT. PANEL INPUTS
HALT
AUD 1 & AUD 2
COIN DOOR OUTPUTS
CONTROL PANEL OUTPUTS
INVERT X
INVERT Y
TO REGULATOR/AUDIO II PCB
TO COIN DOOR
TO CONTROL PANEL
FROM COIN DOOR SWITCHES
FROM CONTROL PANEL SWITCHES
Sheet 5B
Vector Address
Decoder
Vector Read-Only
Memory
Vector Random-
Access Memory
Vector Memory Data
Buffer
Vector Address
Selector
AVG0-AVG12
Sheet 6A
Vector Data Shifters
OP Code and Intensity
Latches
LATCH0-LATCH3
E NORM
DVX3-DVX12 & DVX12
DVY0-DVY12
DVY0-DVY11
OP0-OP2 & OP0-OP2
OP0-OP2 & OP1-OP2
Z0-Z2 & Z1-Z2
Sheet 6B
State Machine
State Machine Clock
State Machine Clock
Logic
Decoder Disable
Vector Address
Controller
Signature Analysis
Flag
GO
HALT
STROBE0-STROBE7
LATCH0-3
Sheet 7A
Normalization Flag
Vector Scaling
Center Flag
Go Flag
Vector Flag
Vector Timer
Halt Flag
DVY8-12 & DVY12
DVX11 & DVX12
VCTR
STAT CLK
CENTER
DISRST
Sheet 7B
Z Intensity
and Blanking
R-G-B Output
DVY0-DVY2,DVY4-DVY7
Z0-Z2,Z1-Z2
RED
BLUE
GREEN
Z OUT
Sheet 8A & 8B
DAC Reference and
Bipolar Current
Sources
X-Axis Output
Y-Axis Output
INVERT X
INVERT Y
DVX3-11 & DVX12
DVY3-DVY11 & DVY12
X OUT
Y OUT
Sheet 12B
Color X-Y Display
Schematic Diagram
GRAVITAR
TM
ATARI
Guide to Gravitar PCB Schematics
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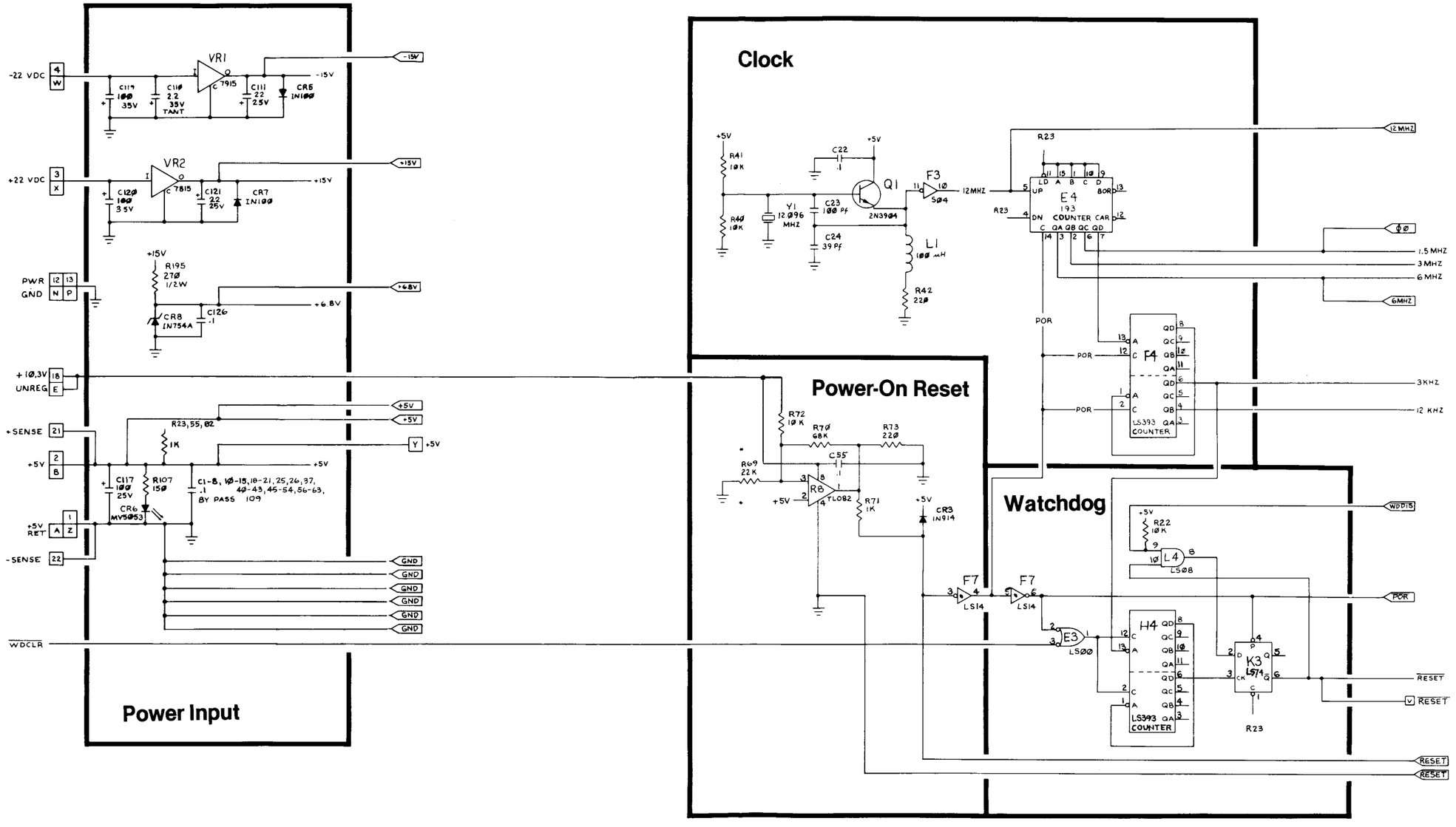

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Gravitar™ PCB Schematic Diagram

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SP-206 Sheet 3B
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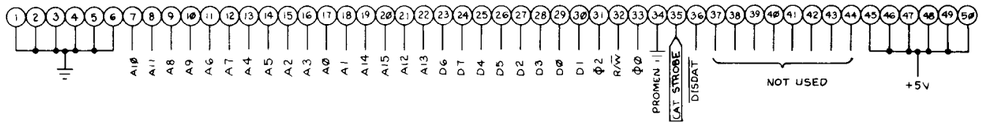
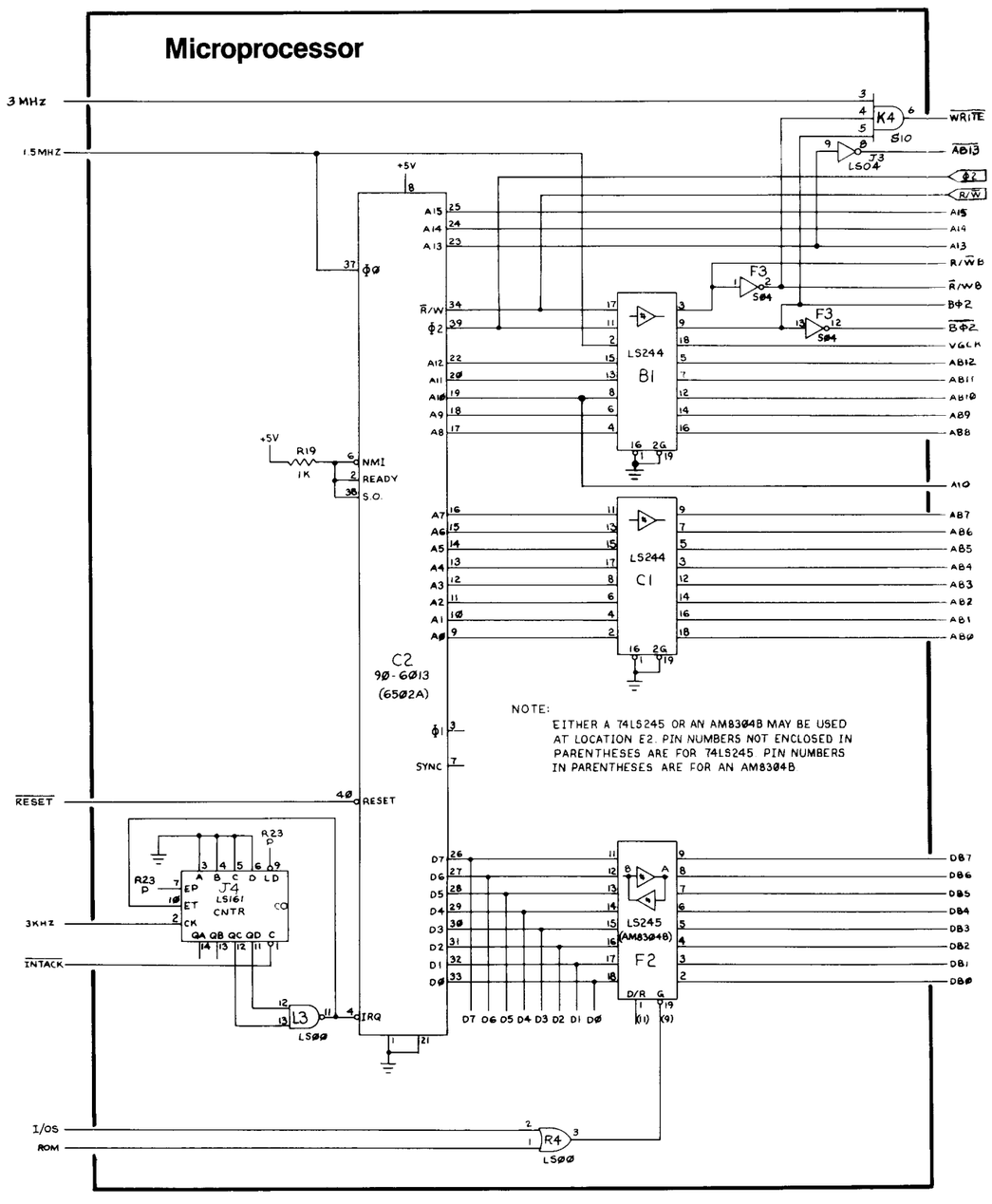
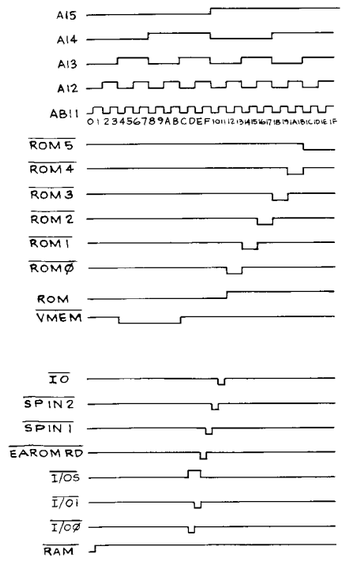
Test Connector



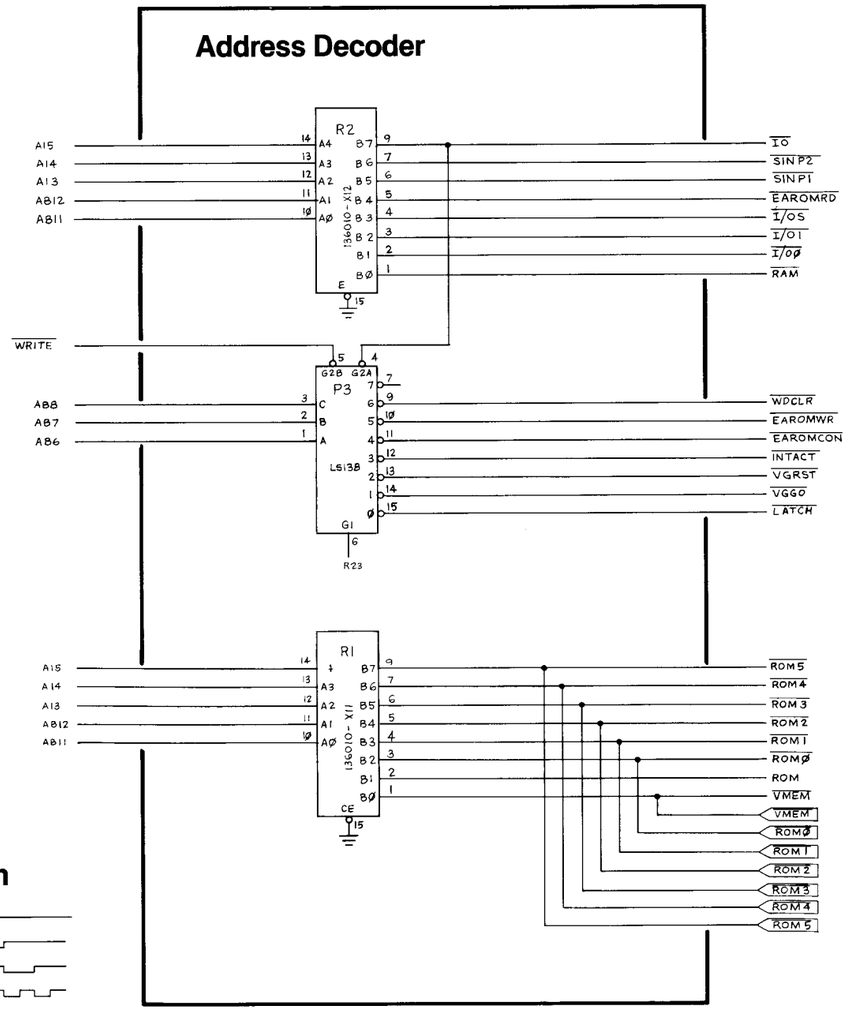
Microprocessor



Timing Diagram



Address Decoder



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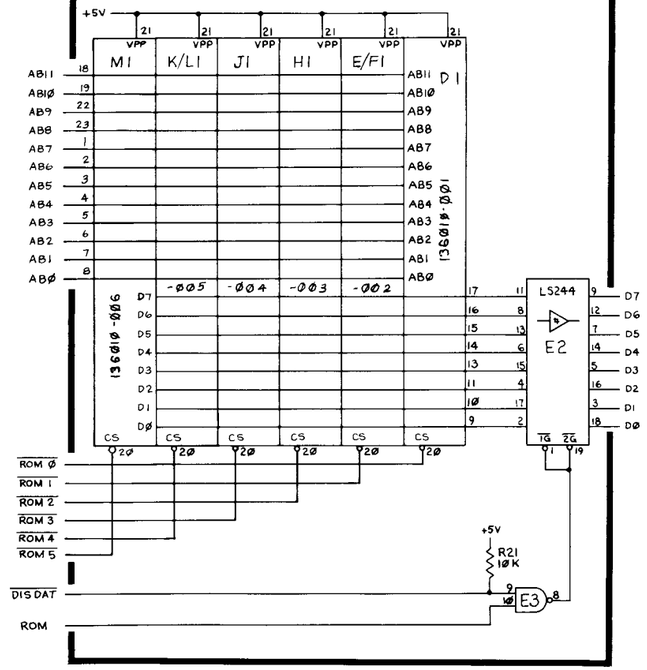
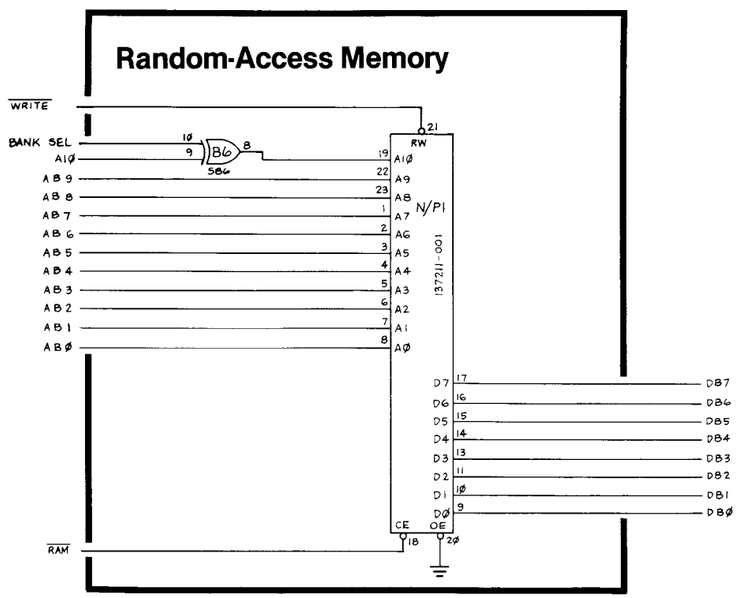
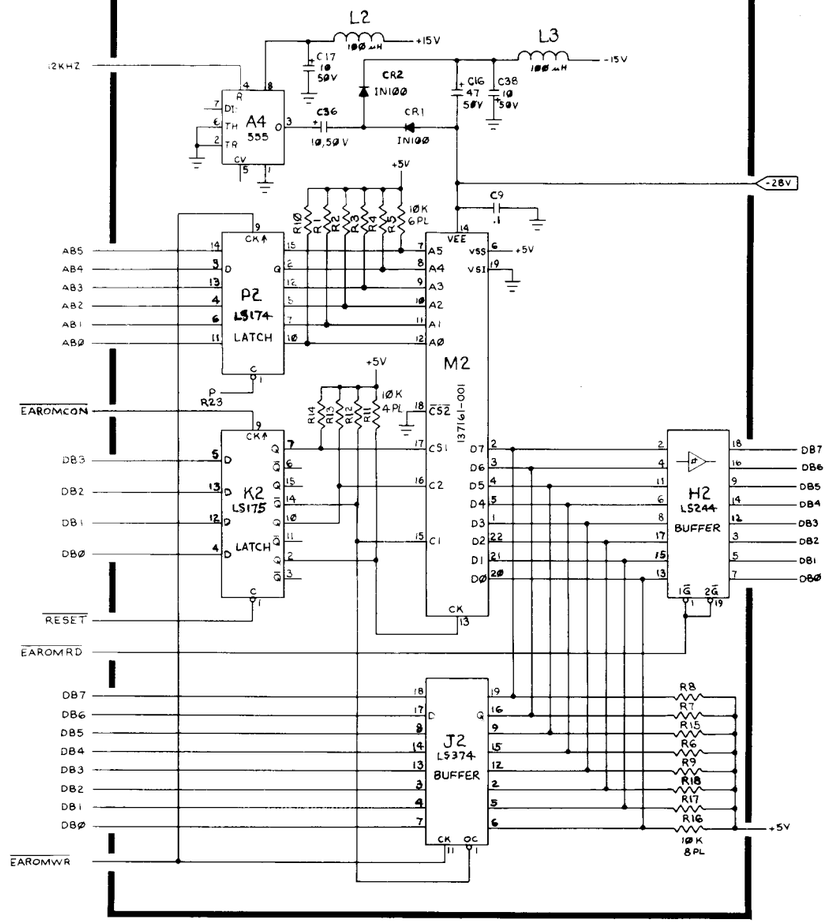
Read-Only Memory



Random-Access Memory



High-Score Table



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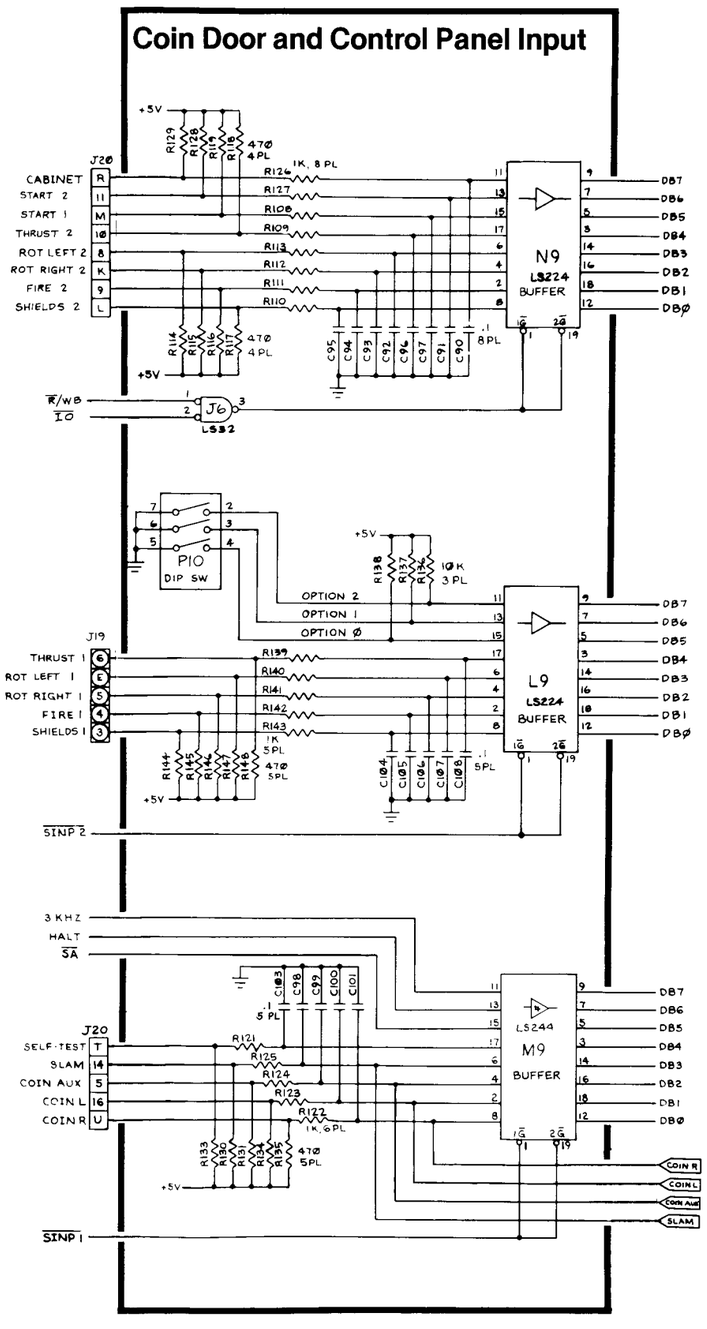
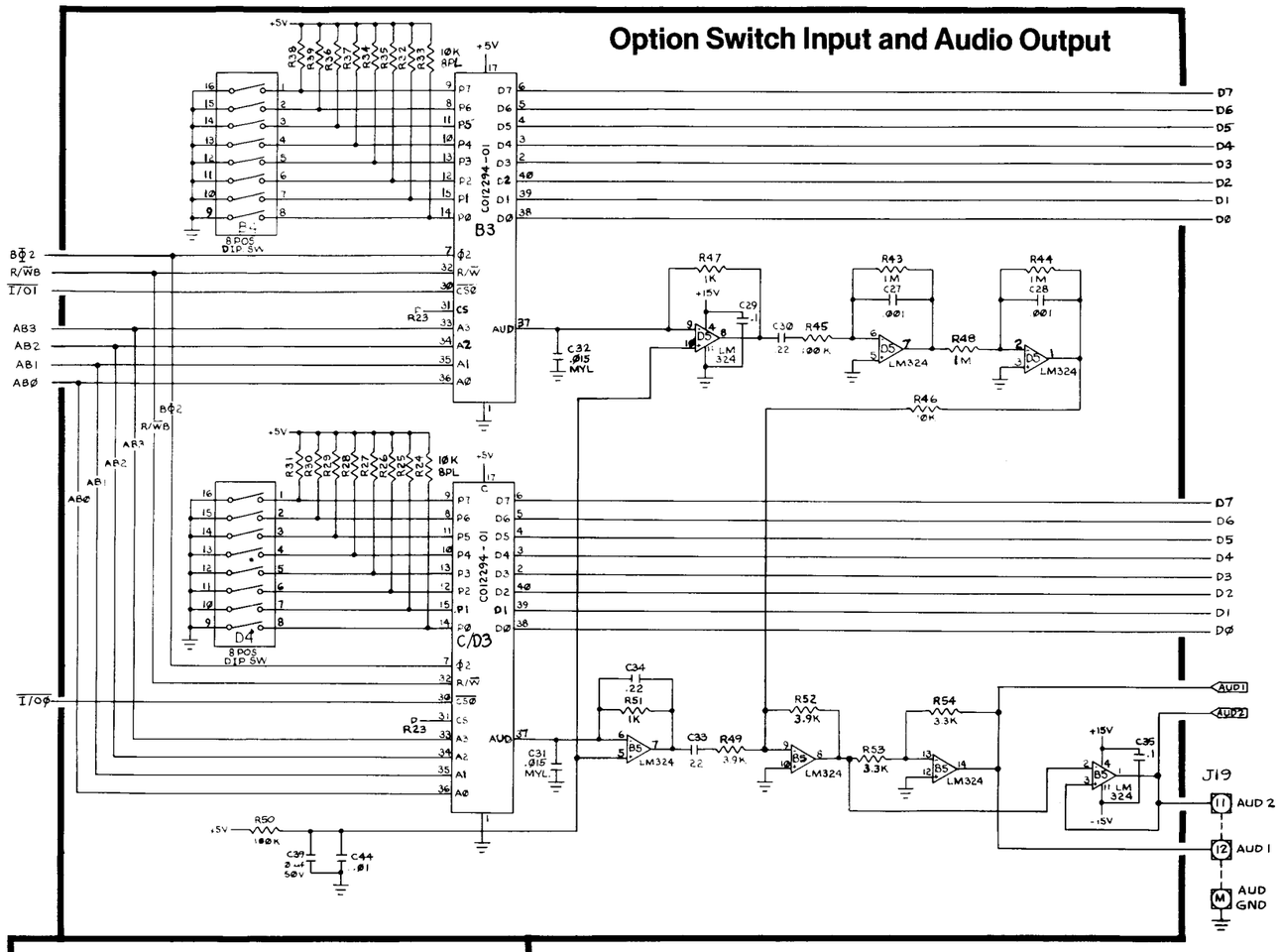
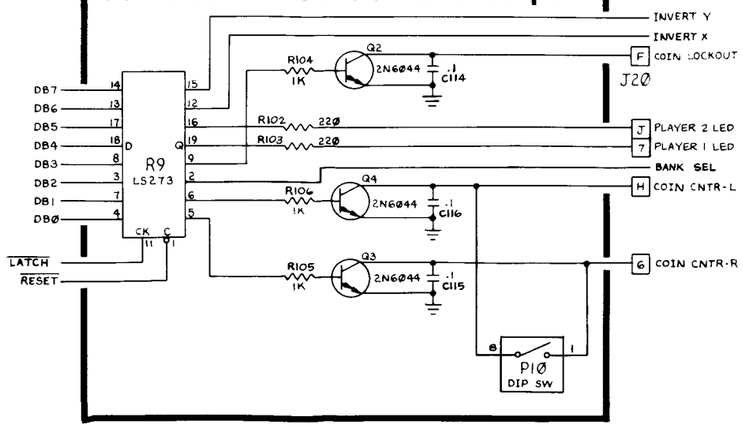
Coin Door and Control Panel Input



Option Switch Input and Audio Output



Coin Door and Control Panel Output



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SP-206 Sheet 5A
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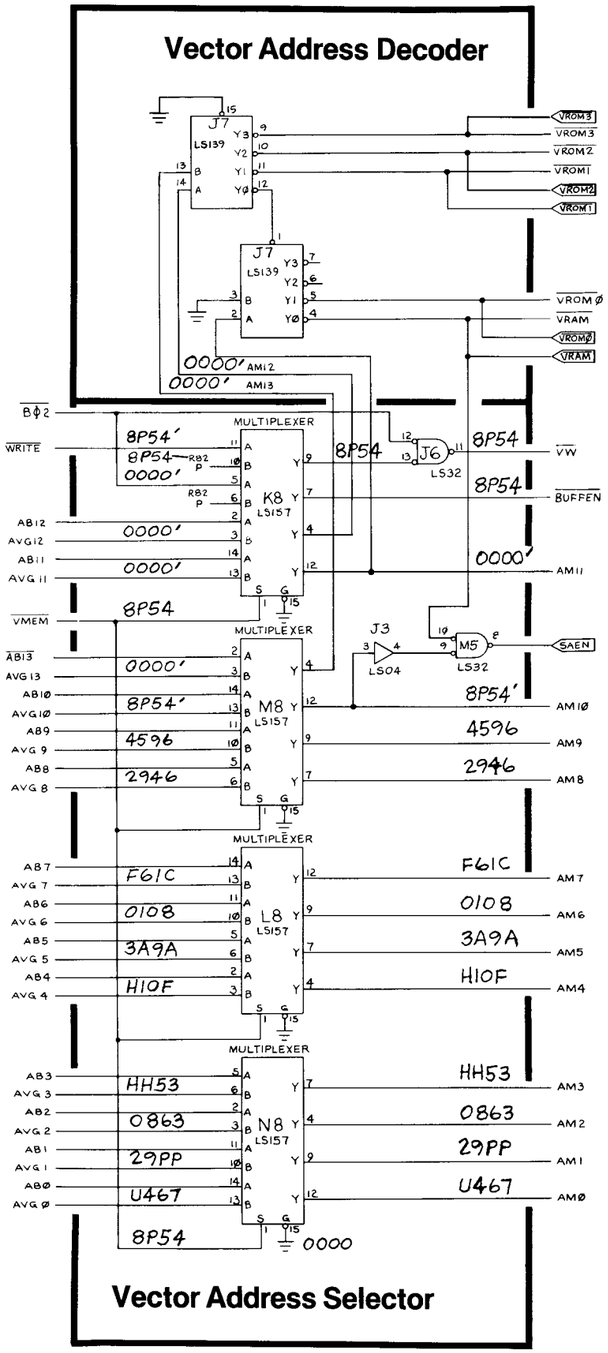
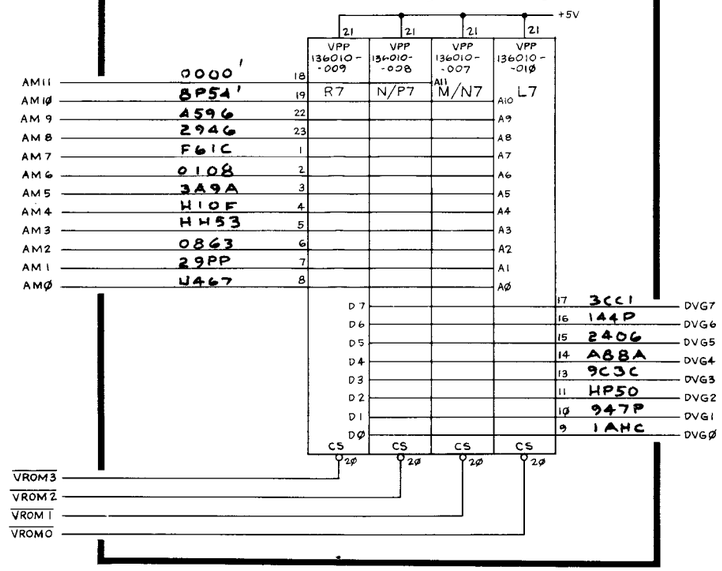
Vector Address Decoder

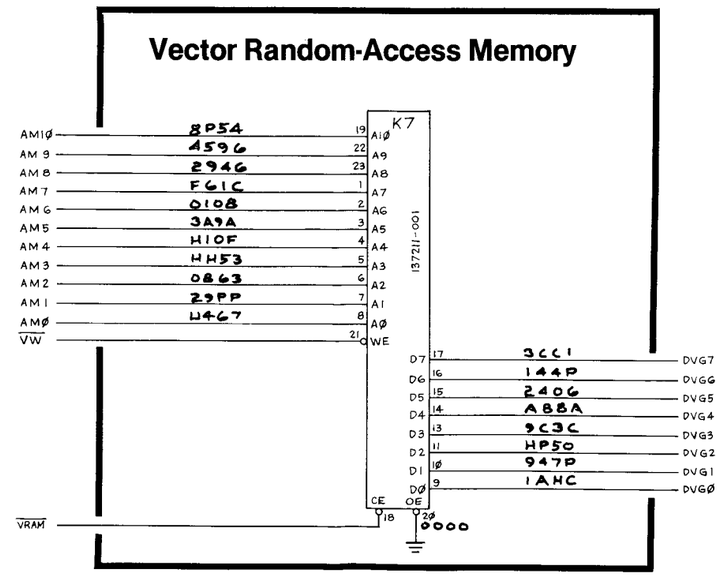


Vector Address Selector

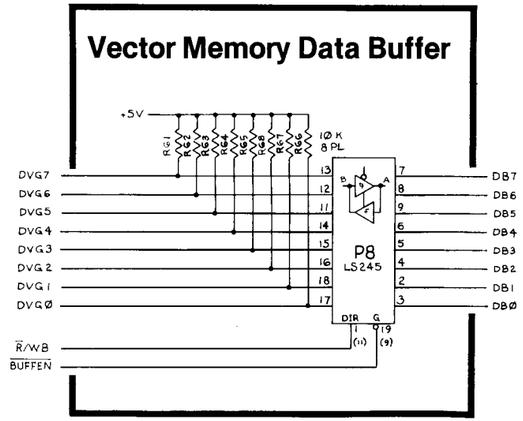
Vector Read-Only Memory



Vector Random-Access Memory



Vector Memory Data Buffer



NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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Gravitar™ PCB Schematic Diagram

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SP-206 Sheet 5B
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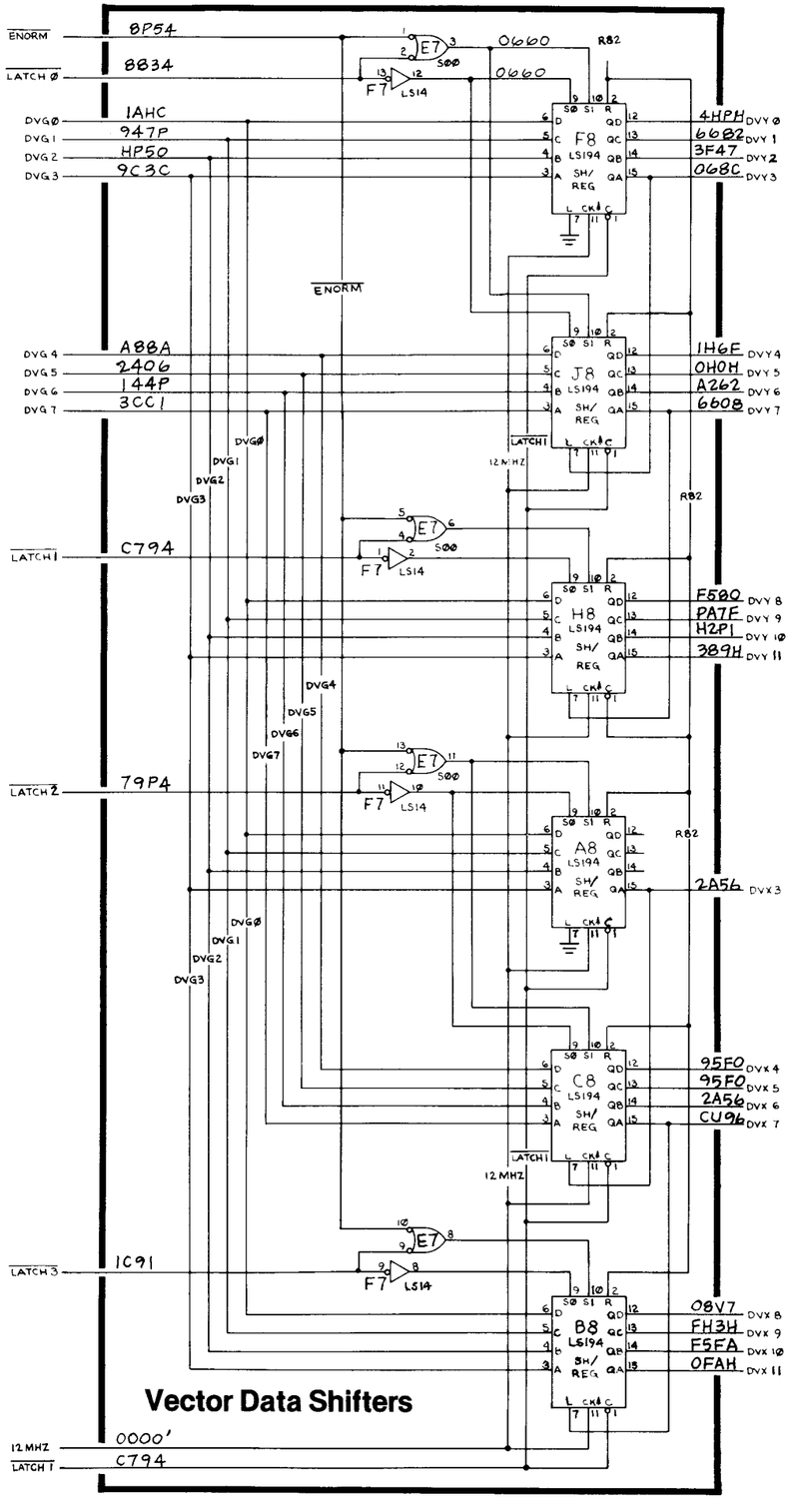

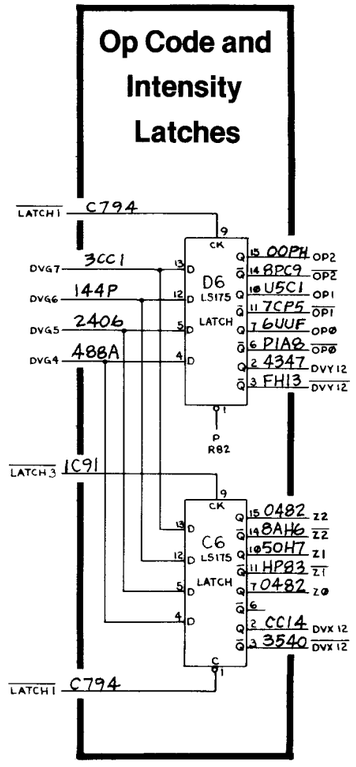

NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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Signature Analysis Flag

Address Controller

State Machine Clock

State Machine Clock Logic

Decoder Disable

State Machine

NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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SP-206 Sheet 6B
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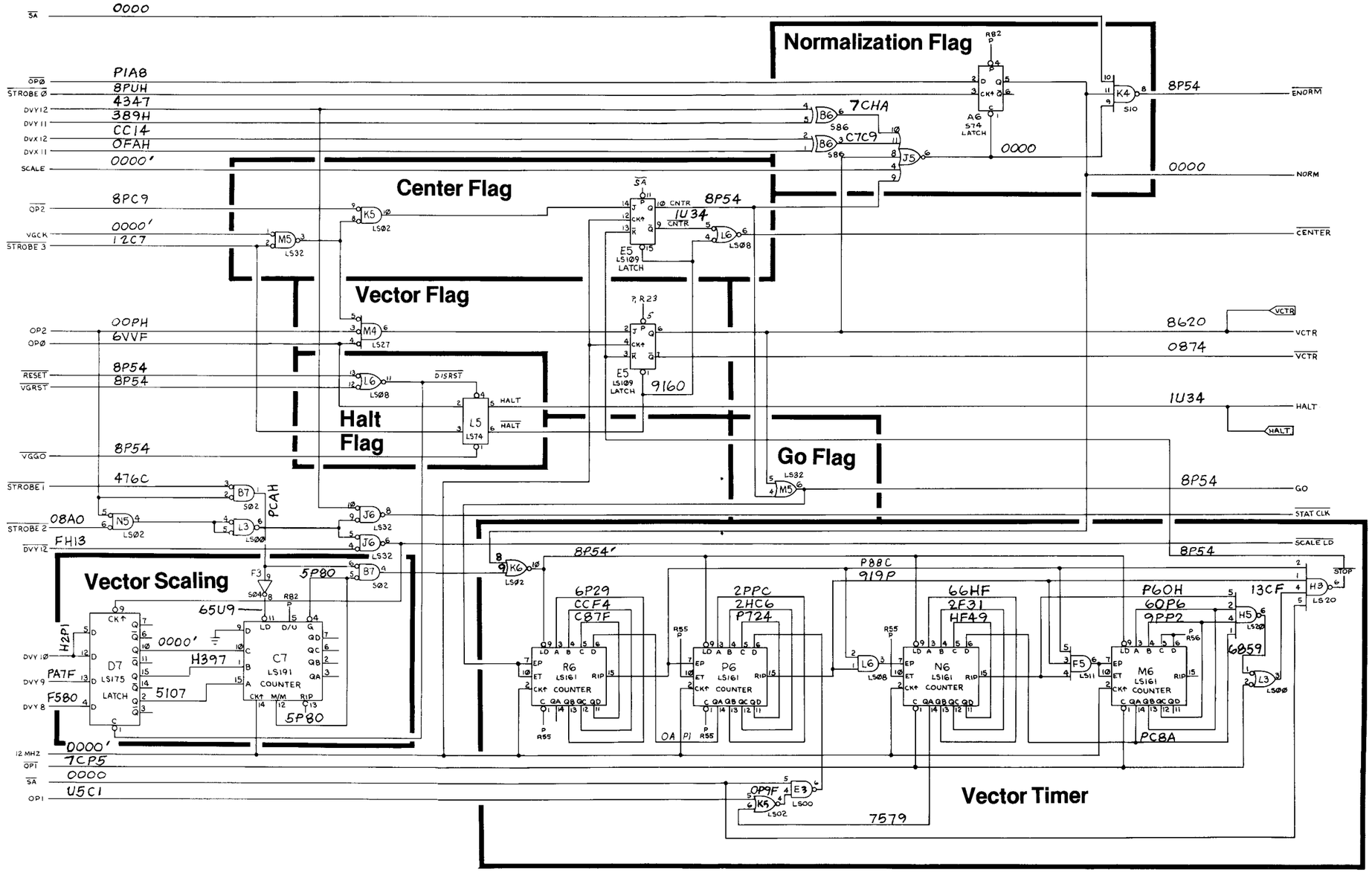

NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.

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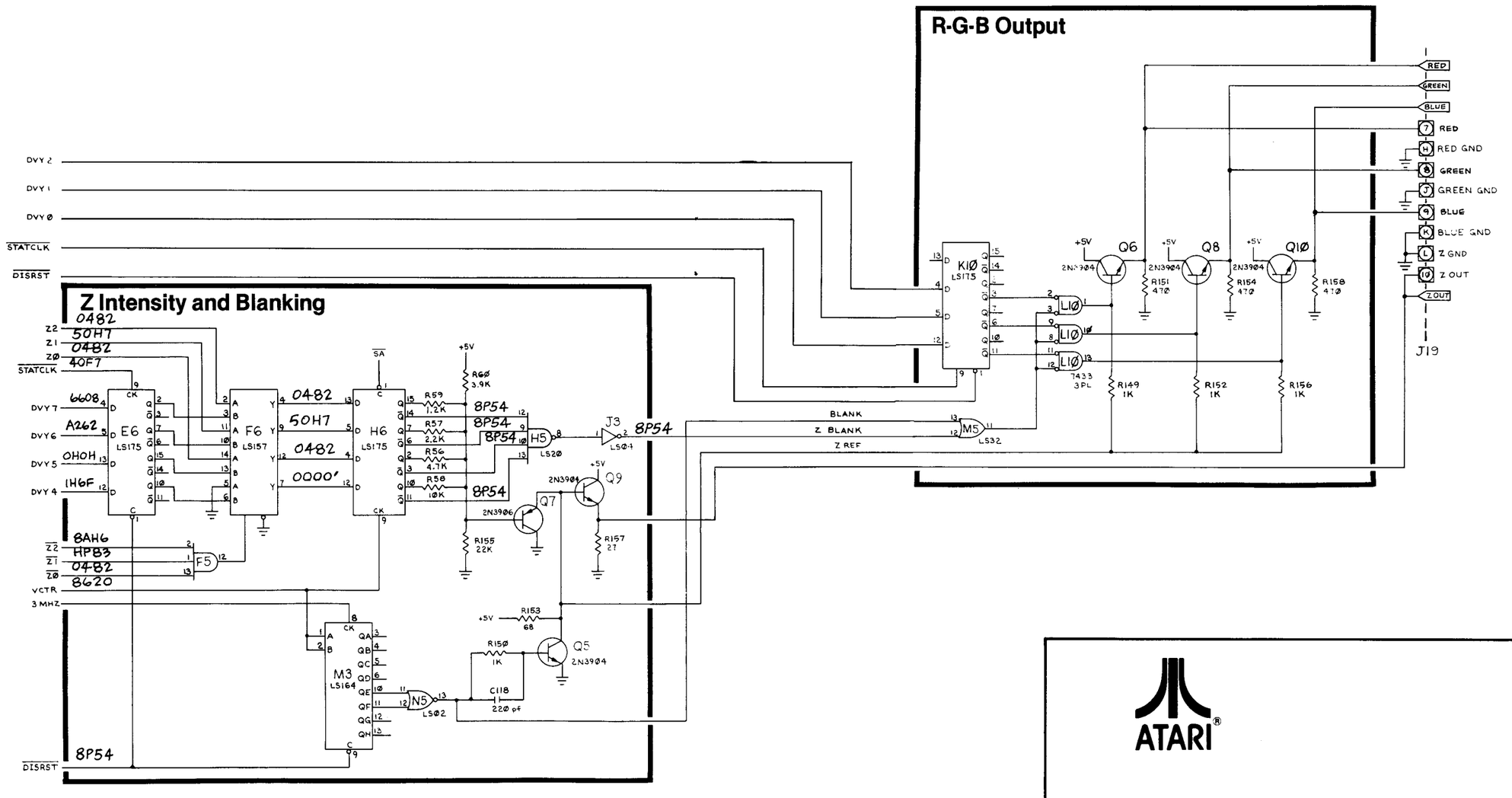
Gravitar™ PCB Schematic Diagram

SP-206 Sheet 7A
1st printing

NOTE:
Signatures enclosed in parentheses should be checked only after all others are correct. Signatures followed by ' are pulsing.



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Gravitar™ PCB Schematic Diagram

SP-206 Sheet 7B
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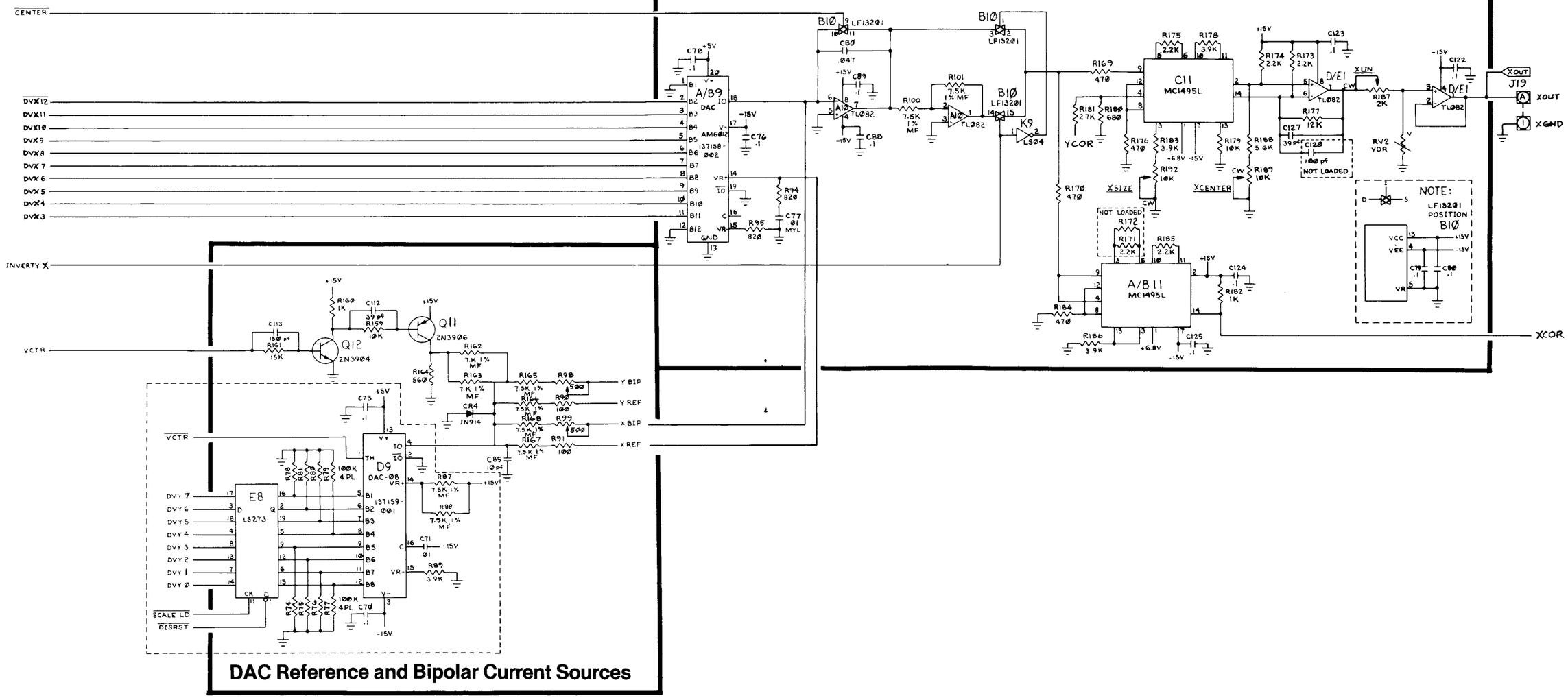
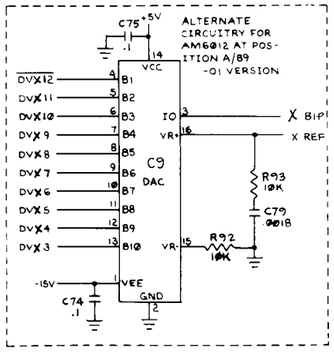
X-Axis Output



DAC Reference and Bipolar Current Sources



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Gravitar™ PCB Schematic Diagram

SP-206 Sheet 8A
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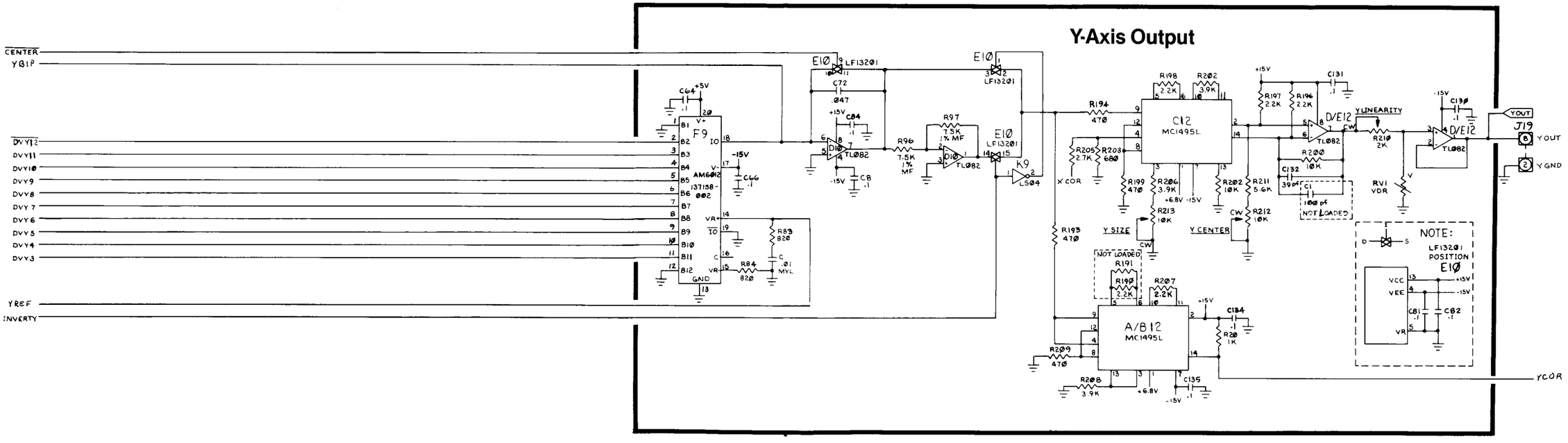

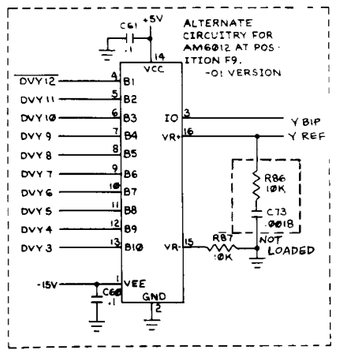

Adjusting X- and Y-Axis Video Potentiometers

If you replace the main Gravitar PCB or the display, you may have to make the following adjustments:

1. Enter self-test and advance to diagonal crosshatch pattern (Screen 2).
2. *Centering Pots:* Adjust X CENTER (R189) and Y CENTER (R212) so that the crosshatch pattern is located at the middle of the screen.
3. *Size Pots:* Adjust XSIZE (R192) and YSIZE (R213) so that the crosshatch pattern exactly covers the whole visible screen.
4. *Linearity Pots:* Adjust XLIN (R187) and YLIN (R210) so that the diagonal lines are straight. Since the LIN pots change the size of the displayed picture on the screen, you may have to readjust the SIZE pots in order to get the correct adjustment.
5. *Bipolar Pots:* Advance to the self-test raster pattern (Screen 4). Adjust XBIP (R99) and YBIP (R98) for a 1-inch high horizontal raster in the center of the screen. Be sure the raster ends are square with the sides of the outer rectangle.

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Gravitar™ PCB Schematic Diagram

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SP-206 Sheet 8B
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Descriptions of Gravitar PCB Signal Names

A10, A13-A15

Address bits on Microprocessor Address Bus lines A10 and A13-A15 are generated by Microprocessor C2. Bits on lines A13-A15, together with those on AB11-AB12, are the input bits to Address Decoders R1-R2. A10 is exclusive-ORed with BANK SEL by gate B6 to produce the A10 input bit for Random-Access Memory N/P1.

AB0-AB12

Address bits on Buffered Microprocessor Address Bus lines AB0-AB12 are software-generated by Microprocessor C2 and buffered by B1 and C1. These signals are the input bits to Read-Only Memories D1, E/F1, H1, J1, K/L1, and M1; and to Random-Access Memory N/P1.

Address bits AB6-AB8 are the select input signals for Address Decoder P3.

Address bits AB11-AB12 and A13-A15 are the input bits for Address Decoders R1 and R2.

Address bits AB0-AB13 are applied with bits from AVG0-AVG12 to Vector Address Selectors K8, M8, L8, and N8 to produce the data on lines AM0-AM12.

Bits AB0-AB3 are control signals to custom audio chips B3 and C/D3 in the Option Switch Input and Audio Output circuit.

Bits AB0-AB5 are the input signals to latch P2 in the High-Score Table circuit where they are used to produce the A1-A5 address input for EAROM M2.

$\overline{AB13}$

$\overline{AB13}$ is from AB13, inverted by J3, and applied to Vector Address Selector M8. When $\overline{VMEM}$ is low, $\overline{AB13}$ and $\overline{AB12}$ select the specific Vector Memory Read-Only Memory.

AM0-AM13

Address bits on Multiplexed Address Bus lines AM0-AM13 are software-generated by Vector Address Selectors K8, L8, M8, and N8. When $\overline{VMEM}$ is low, the Multiplexed Address Bus is from Buffered Microprocessor Address Bus AB0 through AB12 and $\overline{AB13}$. When $\overline{VMEM}$ is high, AM0-AM12 is from Vector-Generator Address Bus lines AVG0-AVG13.

Signals AM0-AM11 are the input address signals to Vector Read-Only Memories L7, M/N7, N/P7, R7 and to Vector Random-Access Memory K7. In addition, AM11-AM13 are the select input signals for Vector Address Decoder J7. AM0-AM7 are input signals for multiplexers N3 and R3 of the State Machine circuit.

AUD 1-AUD 2

The Audio 1 and Audio 2 signals are game PCB output signals that are generated by custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit. AUD 1 is the inverse of AUD 2. These signals are applied to the Audio/Regulator II PCB and ultimately drive speakers 1 and 2.

AVG0-AVG13

Address bits on Vector-Generator Address Bus lines AVG0-AVG13 are software-generated by Vector Address Controller J9. When $\overline{VMEM}$ is high, these signals are passed through the Vector Address Selectors on lines AM0-AM13 to the Vector Read-Only Memory and the Vector Random-Access Memory.

BANK SEL

The Bank Select signal is developed from data on line DB2. When latch R9 of the Coin Door and Control Panel Output circuit is clocked by $\overline{LATCH}$, R9 latches the data on DB2 to pin 2 of R9, producing the BANK SEL signal. BANK SEL is exclusive-ORed with the address bit A10 by gate B6 to produce input address bit A10 for Random-Access Memory N/P1.

BLANK

Blank is an active high-level signal generated by counter M3 in the Z Intensity and Blanking circuit and ORed with Z BLANK by gate M5 of the R-G-B Output circuit. When high, BLANK turns off transistors Q6, Q8, and Q10, which kills the RED, GREEN, and BLUE output signals to the display.

BLUE

Blue is a game PCB output signal developed from the data on line DVY0. When the data bit on DVY0 is high and latch K10 of the R-G-B Output circuit is clocked by $\overline{STATCLK}$, the data on DVY0 is inverted and latched to pin 11 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q10. Transistor Q10 generates the BLUE signal for the display.

$\overline{BUFFEN}$

Buffer Enable is an active low-level signal developed from $\overline{B\Phi2}$ by Vector Address Selector K8. $\overline{BUFFEN}$ is the enable input signal for Vector Memory Data Buffer P8. When low, $\overline{BUFFEN}$ allows P8 to pass data.

BΦ2

The active high-level Phase 2 Clock signal is hardware-generated from the internal clock circuitry of Microprocessor C2, buffered by B1, and applied to AND gate K4. Gate K4 ANDs together BΦ2, R/$\overline{WB}$, and 3 MHz to produce $\overline{WRITE}$. BΦ2 is also used as the clock signal for custom audio chips B3 and C/D3 of the Option Switch Input and Audio Output circuit.

$\overline{B\Phi2}$

The active low-level Phase 2 Clock signal is generated at pin 12 of F3 by inverting BΦ2. $\overline{B\Phi2}$ is applied to Vector Address Selector K8 to produce $\overline{BUFFEN}$.

$\overline{CENTER}$

Center is an active-low level signal software-generated by gating $\overline{CNTR}$ with $\overline{HALT}$ by Center Flag gate L6. When low, $\overline{CENTER}$ closes switches E10 of the Y-Axis Output circuit and B10 of the X-Axis Output circuit to center the beam on the display.

CNTR

The active high-level Center Flag signal is software-generated by latch E5 of the Center Flag circuit. CNTR is set high when VGCK, $\overline{STROBE3}$, and $\overline{OP2}$ are low. CNTR is applied to gate J5 of the Normalization Flag circuit to develop the clear signal for latch A6. CNTR is ORed with VCTR by GO Flag gate M5 to generate the GO signal.

$\overline{CNTR}$

The active low-level Center Flag signal is software-generated by latch E5 of the Center Flag circuit. When clocked by the 12-MHZ signal, E5 latches $\overline{STOP}$ to pin 9 to produce $\overline{CNTR}$. $\overline{CNTR}$ is gated with $\overline{HALT}$ by Center Flag gate L6 to generate $\overline{CENTER}$.

COIN CNTR-L

Coin Counter Left is a game PCB output signal developed from the data bit on line DB1. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB1 to pin 6 of R9. From here, the signal is current amplified and inverted by Q4 and applied to the game Utility Panel to activate the Left Coin Counter.

COIN CNTR-R

Coin Counter Right is a game PCB output signal developed from the data bit on line DB0. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB0 to pin 5 of R9. From here, the signal is current amplified and inverted by Q3 and applied to the game Utility Panel to activate the Right Coin Counter.

COIN LOCKOUT

Coin Lockout is a game PCB output signal developed from the data on line DB3. When clocked by $\overline{LATCH}$, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB3 to pin 9 of R9. From here, the signal is current amplified and inverted by Q2 and applied to the Right and Left Lockout Coils of the game Coin Door.

D0-D7

Microprocessor Data Bus lines D0-D7 form a bi-directional data bus between the Microprocessor, the Read-Only Memory, and the Option Switch Input circuits.

DB0-DB7

Buffered Microprocessor Data Bus lines DB0-DB7 form a buffered bi-directional data bus between microprocessor data-bus buffer F2 and Vector Memory Data Buffer P8; Coin-Door and Control Panel Input circuit buffers L9, M9, and N9; High-Score Table latches K2 and J2; and High-Score Table buffer H2.

$\overline{DIS\ DAT}$

Disable Data is an active low-level signal generated by test equipment connected to the $\overline{DIS\ DAT}$ test point. $\overline{DIS\ DAT}$ is ANDed with the ROM signal by gate E3 to produce the enable signal for buffer E2 of the Read-Only Memory circuit. When enabled, buffer E2 passes data from the selected Read-Only Memory to the Microprocessor Data Bus.

$\overline{DISRST}$

Display Reset is an active low-level signal software-generated by gate L6 of the Halt Flag circuit. When either $\overline{RESET}$ or $\overline{VGRST}$ is low, $\overline{DISRST}$ is set low. When low, $\overline{DISRST}$ clears State Machine latch P4, DAC Reference and Bipolar Current Sources latch E8, R-G-B Output latch K10, Vector Scaling latch D7, Z Intensity and Blanking latch E6 and counter M3. In addition, $\overline{DISRST}$ presets the HALT signal from latch L5 to the high level.

DVG0-DVG7

Data bits on Vector-Generator Data Bus lines DVG0-DVG7 are software-generated by the selected Vector Read-Only Memory or Vector Random-Access Memory. If Vector Memory Data Buffer P8 is enabled ($\overline{BUFFEN}$ is low) and the R/$\overline{WB}$ line is low, the data on lines DVG0-DVG7 is passed through P8 to the Buffered Microprocessor Data Bus to be read by the microprocessor. Otherwise, the data on DVG0-DVG7 is sent to the Vector Data Shifters and to the Op Code and Intensity Latches.

DVX3-DVX12, $\overline{DVX12}$

Data bits on X-Axis Vector Data lines DVX3-DVX12 and $\overline{DVX12}$ are software-generated by Vector Data Shifters A8, B8, C8, and by latch C6 of the Op Code and Intensity Latches circuit. DVX3-DVX11 and $\overline{DVX12}$ are the input signals to digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit. The data carried on these lines represents the X-axis change from the current location of the display beam. If $\overline{DVX12}$ is low, DAC A/B9 operates only in its lower 512 positions, which means a negative direction of change on the display. If $\overline{DVX12}$ is high, DAC A/B9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVX11 and DVX12 are exclusive-ORed by gate B6 of the Normalization Flag circuit.

DVY0-DVY12, $\overline{DVY12}$

Data bits on Y-Axis Vector Data lines DVY0-DVY12 and $\overline{DVY12}$ are software-generated by Vector Data Shifters F8, H8, J8, and by latch D6 of the Op Code and Intensity Latches circuit. DVY3-DVY11 and $\overline{DVY12}$ are the input signals for digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit. The data carried on these lines represents the Y-axis change from the current location of the display beam. If $\overline{DVY12}$ is low, DAC F9 operates only in its lower 512 positions, which means a negative direction of change on the display. If $\overline{DVY12}$ is high, DAC F9 operates only in its upper 512 positions for a positive direction of change on the display.

In addition, DVY0-DVY7 are applied to latch E8 in the DAC Reference and Bipolar Current Sources circuit. These signals, together with VCTR and $\overline{VCTR}$, set the X REF and Y REF voltage levels (via DAC D9).

Lines DVY0-DVY2 carry data representing the eight different color signals for latch K10 of the R-G-B Output circuit.

Lines DVY4-DVY7 carry data representing the Z-intensity signals for latch E6 of the Z Intensity and Blanking circuit.

Data on DVY8-DVY10 are applied to latch D7 of the Vector Scaling circuit. The data carried on these lines represents the number (in binary) that the Vector Scaling circuit uses to divide into the vector drawing time. The vector drawing time n is divided by 2 , where n equals the number represented on DVY8-DVY10.

In addition, DVY11 and DVY12 are exclusive-ORed by gate B6 of the Normalization Flag circuit.

$\overline{EAROMCON}$

The Electrically-Alterable ROM Control signal is an active low-level signal software-generated by Address Decoder P3 at address 8900. $\overline{EAROMCON}$ is the clock signal for latch K2 in the High-Score Table circuit. $\overline{EAROMCON}$ allows K2 to pass data bits on lines DB0-DB3 to the control lines of EAROM M2.

$\overline{EAROMRD}$

The Electrically-Alterable ROM Read Enable is an active low-level signal software-generated by Address Decoder R2 at address 7000. $\overline{EAROMRD}$ is the read-enable signal for buffer H2 of the High-Score Table circuit. $\overline{EAROMRD}$ allows the eight data bits from EAROM M2 to be passed through buffer H2 to the microprocessor data bus.

$\overline{EAROMWR}$

The Electrically-Alterable ROM Write Enable is an active low-level signal software-generated by Address Decoder P3 at address 8940. $\overline{EAROMWR}$ is the clock signal for latches J2 and P2 in the High-Score Table circuit. $\overline{EAROMWR}$ allows address bits on lines AB0-AB5 and data bits on lines DB0-DB7 to pass to the address and data input pins of EAROM M2.

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Gravitar™ PCB Signal Name Descriptions

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Description of Gravitar PCB Signal Names (continued)

ENORM

The active low-level Normalization Flag is software-generated by gate K4 of the Normalization Flag circuit. If OP0 is high, SA is high, and the output from gate J5 is high, ENORM is set low when STROBE0 goes high. ENORM is applied through gate E7 to the S1 input pins of Vector Data Shifters A8, B8, C8, F8, H8, and J8. ENORM multiples the rate of change of the X and Y vector data in the Vector Data Shifters (via shift left operations) at the same 2^n factor specified by data on lines DVY8-DVY10. The n number is incremented at a 12-MHz rate until either DVX11 or DVY11 changes state, which then sets ENORM to the high level.

GO

The Go flag is an active high-level signal software-generated by gate M5 of the Go Flag circuit when either VCTR or CNTR are high. GO is gated with HALT* by gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM N4.

GO is also used as the enable signal for Vector Timer R6. When GO is high, the Vector Timer starts its count. The Vector Timer counts to 256 if OP1 is high and OP1 is low. If OP1 is low and OP1 is high, the Vector Timer counts to 16K.

GREEN

Green is a game PCB output signal developed from the data on line DVY1 in the R-G-B Output circuit. When DVY1 is high and latch K10 is clocked by STATCLK, the data bit on DVY1 is inverted and latched to pin 6 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q8. Transistor Q8 generates the GREEN signal for the display.

HALT

The active high-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. HALT is applied through buffer M9 of the Coin Door and Control Panel Input circuit (when SINP1 is low) to permit Microprocessor C2 to read the status of HALT on line DB6. In addition, HALT is applied to latch P4 of the State Machine circuit to develop HALT*.

HALT*

The active high-level Delayed Halt Flag is software-generated by latch P4 of the State Machine circuit. HALT* is generated when the HALT signal has been delayed by one pulse of inverted VGCK (1.5 MHz), which in turn has been delayed by one pulse of 12 MHz. HALT* is ORed with GO by gate N5 of the State Machine circuit to produce the A7 input address bit for State Machine ROM N4.

HALT

The active low-level Halt Flag is software-generated by latch L5 of the Halt Flag circuit. HALT is the clear signal for Vector Flag latch E5 and Center Flag latch E5. In addition, HALT is ORed with CNTR by gate L6 of the Center Flag circuit to produce CENTER.

INTACK

Interrupt Acknowledge is an active low-level signal software-generated from Address Decoder P3 at address 88C0. This signal is an acknowledgment from Microprocessor C2 that an interrupt request has been received. INTACK resets counter J4.

INVERT X

Invert X is an active high-level signal developed from the data bit on line DB6. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB6 to pin 12 of R9. When high, INVERT X closes switch B10 through inverter K9 in the X-Axis Output circuit. This inverts the X-axis vector instruction to the display.

INVERT Y

Invert Y is an active high-level signal developed from the data bit on line DB7. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches DB7 to pin 15 of R9. When high, INVERT Y closes switch E10 through inverter K9 in the Y-Axis Output circuit. This inverts the Y-axis vector instruction to the display.

IO

The Input/Output signal is an active low-level signal software-generated by Address Decoder R2 during addresses 8000 through 8FFF. IO is gated with R/WB by gate J6 to produce the direction signal for bi-directional data buffer N9 of the Coin Door and Control Panel Input circuit. IO determines the direction of data flow through buffer N9.

I/OS

I/OS is an active high-level signal software-generated from Address Decoder R2 during addresses 6000 through 6FFF. The I/OS signal is ORed with the ROM signal by gate R4 to enable bi-directional data bus buffer F2 to pass data. When I/OS is high, data buffer F2 is turned off, which allows custom audio chips B3 and C/D3 to pass data to the data bus.

I/O0

I/O0 is an active low-level signal software-generated by Address Decoder R2 at address 6800. I/O0 is the chip-select enable for custom audio chip C/D3 in the Option Switch Input and Audio Output circuit.

I/O1

I/O1 is an active low-level signal software-generated by Address Decoder R2 at address 6000. I/O1 is the chip-select enable for custom audio chip B3 in the Option Switch Input and Audio Output circuit.

LATCH

Latch is an active low-level signal generated by Address Decoder P3 at address 8800. LATCH is the clock signal for latch R9 in the Coin Door and Control Panel Output circuit. When low, LATCH allows the data bits on lines DB0-DB7 to pass through R9.

LATCH0

Latch 0 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH0 is applied through inverter F7 to the S0 input pins of shift registers F8 and J8 in the Vector Data Shifters circuit. LATCH0 causes the data bits on lines DVG0-DVG7 to be latched by F8 and J8 to lines DVY0-DVY7 when F8 and J8 are clocked by the 12-MHz clock signal.

LATCH1

Latch 1 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH1 is applied through inverter F7 to the S0 input pin of shift register H8 in the Vector Data Shifters circuit. LATCH1 causes the data bits on lines DVG0-DVG3 to be latched by H8 to lines DVY8-DVY10 when H8 is clocked by the 12-MHz clock signal.

LATCH1 is also the clear signal for Vector Data Shifters A8, B8, C8, F8, J8, and for Op Code and Intensity Latch C6.

In addition, LATCH1 is the clock signal for Op Code and Intensity Latch D6. When LATCH1 goes low, the data bits on lines DVG4-DVG7 are latched by D6 to lines OP0-OP2, OP0-OP2, DVY12, and DVY12.

LATCH2

Latch 2 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH2 is applied through inverter F7 to the S0 input pins of shift registers A8 and C8 in the Vector Data Shifters circuit. LATCH2 causes the data bits on lines DVG0-DVG7 to be latched by A8 and C8 to lines DVX3-DVX7 when A8 is clocked by the 12-MHz clock signal.

LATCH3

Latch 3 is an active low-level signal software-generated by decoder H7 of the State Machine circuit. LATCH3 is applied through inverter F7 to the S0 input pin of shift register B8 in the Vector Data Shifters circuit. LATCH3 causes the data bits on lines DVG0-DVG3 to be latched by B8 to lines DVX8-DVX11 when B8 is clocked by the 12-MHz clock signal.

LATCH3 is also the clock signal for Op Code and Intensity Latch C6. When LATCH3 goes low, the data bits on lines DVG4-DVG7 are latched by C6 to lines Z0-Z2, Z1-Z2, DVX12, and DVX12.

NORM

The active high-level Normalization Flag is software-generated by latch A6 in the Normalization Flag circuit. If OP0 is high, NORM is set high when STROBE0 goes high. NORM is gated with SCALE by gate K5 in the Vector Timer circuit to produce the load-enable signal for Vector Timers M6, N6, P6, and R6. If the Vector Timers are enabled, NORM initiates the divide-by-2^n operation of the vector drawing time. (The n factor is specified by the data on lines DVY8-DVY10 to Vector Scaling latch D7.)

OPTION 0-OPTION 2

The Option 0, Option 1, and Option 2 signals are hardware-generated by DIP switch P10. They are applied to switch input buffer L9 of the Coin Door and Control Panel Input circuit. When L9 is enabled by SINP2, OPTION 0-OPTION 2 are passed to Buffered Microprocessor Data Bus lines DB5-DB7.

OP0

The Op Code 0 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG5 is high, OP0 is set high when D6 is clocked by LATCH1. OP0 is multiplexed with AM4 by N3 in the State Machine circuit to produce the A4 input address bit for State Machine ROM N4.

If OP0 is high, HALT from Halt Flag latch L5 is set high when L5 is clocked by STROBE3.

If OP0, OP2, STROBE3, and VGCK are all low, VCTR from Vector Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

OP0

The Complementary Op Code 0 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP0. If OP0 is low, NORM from Normalization Flag latch A6 is set high when STROBE0 clocks A6. OP0 is also the OP0 and OPX input signal for Vector Address Controller J9.

OP1

The Op Code 1 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG6 is high, OP1 is set high when D6 is clocked by LATCH1. OP1 is multiplexed with AM5 by N3 in the State Machine circuit to produce the A5 input address bit for State Machine ROM N4. In addition, OP1 is the OP1 signal for Vector Address Controller J9.

In the Vector Timer circuit, OP1 is gated by K5 and E3 to enable a 1 to be loaded into the D input pin of Vector Timer P6 (if NORM or SCALE is low).

OP1

The Complementary Op Code 1 signal is sofware-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP1. OP1 is the clear signal for Vector Timers N6 and M6. When OP1 goes low, the count from N6 and M6 is stopped, causing a lowered count from the Vector Timer circuit. This low count is used to draw short vectors on the display. OP1 is also gated with the outputs of the Vector Timers by gates L3 and H3 to set STOP to the low level.

OP2

The Op Code 2 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. If the data on line DVG7 is high, OP2 is set high when D6 is clocked by LATCH1. OP2 is multiplexed with AM6 by N3 in the State Machine circuit to produce the A6 input address bit for State Machine ROM N4.

If OP2, OP0, STROBE3, and VGCK are all low, VCTR from Vector Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal.

When STROBE1 goes low, if OP2 is low, it is applied through gates B7 and F3 of the Vector Scaling circuit as the load signal for counter C7. This allows the data latched from DVY8-DVY10 by D7 to be loaded into counter C7. When STROBE1 goes high, counter C7 counts down until it reaches the minimum count. At the same time, the Vector Timer circuit does a divide-by-2 (shift right) operation for each count of C7. (This is caused by SCALE being at the high state.) When C7 reaches its minimum count, it sets pin 12 high, dropping SCALE to the low state.

If OP2 and DVY12 are low, SCALELD from gate J6 is set low when STROBE2 goes low. This allows Vector Scaling latch D7 to latch the new data on DVY8-DVY10.

If OP2 and DVY12 are low, STATCLK from J6 is set low when STROBE2 goes low. This allows latch E6 of the Z Intensity and Blanking circuit to latch the data on DVY4-DVY7.

OP2

The Complementary Op Code 2 signal is software-generated by latch D6 in the Op Code and Intensity Latches circuit. This signal is opposite in state to OP2. If OP2, STROBE3, and VGCK are low, CNTR from Center Flag latch E5 is set high when E5 is clocked by the 12-MHz clock signal. OP2 is also ORed with SA by gate R4 to produce the OP2 input for Vector Address Controller J9.

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Gravitar™ PCB Signal Name Descriptions

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Description of Gravitar PCB Signal Names (continued)

PLAYER 1 LED

The Player 1 LED On signal is developed from the data bit on line DB4. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on line DB4 to pin 19 of R9. This signal is applied through R103 to light the Player 1 LED on the game Control Panel.

PLAYER 2 LED

The Player 2 LED On signal is developed from the data bit on line DB5. When clocked by LATCH, latch R9 of the Coin Door and Control Panel Output circuit latches the data bit on DB5 to pin 16 of R9. This signal is applied through R102 to light the Player 2 LED on the game Control Panel.

POR

The active high-level Power-On Reset signal is hardware-generated at pin 4 of F7 in the Power-On Reset circuit. POR is the clock signal that starts the count of E4 of the Clock circuit.

$\overline{\text{POR}}$

The active low-level Power-On Reset signal is hardware-generated at pin 6 of inverter F7 in the Power-On Reset circuit. $\overline{\text{POR}}$ is generated when the voltage at pin 3 of R8 is less than about 7 volts or when the RESET test point is shorted to ground. $\overline{\text{POR}}$ is developed into the $\overline{\text{RESET}}$ signal to protect Microprocessor C2.

$\overline{\text{RAM}}$

The Random-Access Memory Enable is an active low-level signal software-generated by Address Decoder R2 during addresses 0000 through 07FF. $\overline{\text{RAM}}$ is the chip-enable signal for Random-Access Memory N/P1. When low, $\overline{\text{RAM}}$ allows data to be read from or written to N/P1, depending upon the state of $\overline{\text{WRITE}}$.

RED

Red is a game PCB output signal developed from the data on line DVY2 in the R-G-B Output circuit. When DVY2 is high and latch K10 is clocked by $\overline{\text{STATCLK}}$, the data bit on DVY2 is inverted and latched to pin 3 of K10. If both BLANK and Z BLANK are low, this data bit is again inverted by gate L10 to turn on Q6. Transistor Q6 generates the RED signal for the display.

$\overline{\text{RESET}}$

Reset is an active low-level signal generated at pin 6 of K3 from either the Watchdog circuit or the Power-On Reset circuit. The Power-On Reset circuit sets $\overline{\text{RESET}}$ to an active low level either when the RESET test point is shorted to ground or during the time that the power-supply voltages are reaching their stabilized, regu-lated levels. This ensures that the Microprocessor Address Bus is stabilized before the microprocessor begins operation.

The Watchdog circuit sets $\overline{\text{RESET}}$ to an active low level if the microprocessor fails to output address 0D00 before Watchdog counter H4 has reached its maximum count.

$\overline{\text{RESET}}$ is also the clear signal for latch R9 in the Coin Door and Control Panel Output circuit.

In addition, RESET is gated with $\overline{\text{VGRST}}$ by gate L6 in the Halt Flag circuit to produce $\overline{\text{DISRST}}$.

ROM

The Read-Only Memory Enable is an active high-level signal software-generated from Address Decoder R1 during addresses 9000 through 9FFF. ROM is ORed with $\overline{\text{I/OS}}$ by gate R4 to enable bi-directional data bus buffer F2 to pass data.

In addition, ROM is ANDed with $\overline{\text{DIS DAT}}$ to enable data buffer E2.

$\overline{\text{ROM0}}$

Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Address Decoder R1 at addresses 9000-9FFF. $\overline{\text{ROM0}}$ is the chip-select signal for ROM D1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM0}}$ allows ROM D1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM1}}$

Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Address Decoder R1 at addresses A000-AFFF. $\overline{\text{ROM1}}$ is the chip-select signal for ROM E/F1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM1}}$ allows ROM E/F1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM2}}$

Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Address Decoder R1 at addresses B000-BFFF. $\overline{\text{ROM2}}$ is the chip-select signal for ROM H1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM2}}$ allows ROM H1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM3}}$

Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Address Decoder R1 at addresses C000-CFFF. $\overline{\text{ROM3}}$ is the chip-select signal for ROM J1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM3}}$ allows ROM J1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM4}}$

Read-Only Memory Chip Select 4 is an active low-level signal software-generated by Address Decoder R1 at addresses D000-DFFF. $\overline{\text{ROM4}}$ is the chip-select signal for ROM K/L1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM4}}$ allows ROM K/L1 to be addressed and to pass data to buffer E2.

$\overline{\text{ROM5}}$

Read-Only Memory Chip Select 5 is an active low-level signal software-generated by Address Decoder R1 at addresses E000-EFFF. $\overline{\text{ROM5}}$ is the chip-select signal for ROM M1 of the Read-Only Memory circuit. When low, $\overline{\text{ROM5}}$ allows ROM M1 to be addressed and to pass data to buffer E2.

R/$\overline{\text{WB}}$

The Buffered Read/Write Enable is generated by Microprocessor C2, buffered by B1, and applied as the read/write enable signal for custom audio chips B3 and C/D3 of the Option System Input and Audio Output circuit. In the high state, R/$\overline{\text{WB}}$ is the read enable for the custom audio chips; in the low state, it is the write enable for these chips.

$\overline{\text{R}}$/WB

The Buffered Read/Write Eanble is generated at pin 2 of F3 in the Microprocessor circuit by inverting R/$\overline{\text{WB}}$. $\overline{\text{R}}$/WB is ANDed with BΦ2 and 3 MHz by gate K4 to produce $\overline{\text{WRITE}}$. $\overline{\text{R}}$/WB is the direction signal for Vector Memory Data Buffer P8 and determines the direction of data flow through P8. In the high state, $\overline{\text{R}}$/WB allows data to pass through P8 from the data bus to the vector generator data bus; in the low state, it allows data to pass in the reverse direction.

SA

The active high-level Signature Analysis Flag signal is hardware-generated at pin 12 of inverter J3 when test point $\overline{\text{SA}}$ at pin 13 is grounded. SA is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

$\overline{\text{SA}}$

The active low-level Signature Analysis Flag is hardware-generated when test point $\overline{\text{SA}}$ at pin 13 of J3 is grounded. $\overline{\text{SA}}$ is used to place the game PCB in the mode to generate signatures for reading by a Signature Analyzer or the ATARI CAT Box.

SACLK

Signature Analysis Clock is a test point at pin 8 of gate B7 in the State Machine Clock Logic circuit. SACLK is used to apply the clock signal from the Signature Analyzer or ATARI CAT Box for the reading of game PCB signatures.

SAEN

Signature Analysis Enable is a test point at pin 8 of gate M5 in the Vector Address Selector circuit. SAEN is generated by gating $\overline{\text{VRAM}}$ with the data bit on line AM10 by gates J3 and M5. SAEN is used to enable a Signature Analyzer or the ATARI CAT Box for the reading of game PCB signatures.

SCALE

Scale is an active high-level signal generated by gate B7 of the Vector Scaling circuit. When OP2 is high and counter C7 is counting down, SCALE is set high. SCALE is ORed with NORM by gate K5 of the Vector Timer circuit to produce the load signal for Vector Timers M6, N6, P6, and R6. When SCALE is high, the Vector Timers perform a load operation for each count of C7 (at a 12-NHz rate). This results in a vector drawing time divided by a factor of 2^n, where n equals the total counts of C7. When C7 reaches its minimum count, SCALE is set low.

SCALE is gated with VCTR, CNTR, DVY11-DVY12, and DVX11-DVX12 of the Normalization Flag circuit to produce the clear signal for latch A6.

$\overline{\text{SCALELD}}$

Scale Load is an active low-level signal software-generated by gates N5, L3, and L6 of the Vector Generator circuit. When $\overline{\text{STROBE2}}$, OP2, and $\overline{\text{DVY12}}$ are all low, $\overline{\text{SCALELD}}$ is set low. $\overline{\text{SCALELD}}$ is the clock signal for Vector Scaling latch D7. When $\overline{\text{SCALELD}}$ goes high, the data on lines DVY8-DVY10 are latched to the output pins of D7.

$\overline{\text{SINP1}}$

Switch Input 1 is an active low-level signal software-generated by Address Decoder R2 at address 7800. $\overline{\text{SINP1}}$ is the direction signal for bi-directional data buffer M9 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer M9.

$\overline{\text{SINP2}}$

Switch Input 2 is an active low-level signal software-generated by Address Decoder R2 at address 8000. $\overline{\text{SINP2}}$ is the direction signal for bi-directional data buffer L9 of the Coin Door and Control Panel Input circuit and determines the direction of data flow through buffer L9.

$\overline{\text{STATCLK}}$

State Clock is an active low-level signal software-generated by gates N5, L3, and J6 of the Vector Generator circuit. When $\overline{\text{STROBE2}}$, OP2, and DVY12 are all low, $\overline{\text{STATCLK}}$ is set low. $\overline{\text{STATCLK}}$ is the clock for latch K10 in the R-G-B Output circuit and latch E6 in the Z Intensity and Blanking circuit. When $\overline{\text{STATCLK}}$ goes high, the data bits on DVY0-DVY2 are latched by K10, and those on DVY4-DVY7 are latched by E6.

$\overline{\text{STOP}}$

Stop is an active low-level signal generated by gate H3 of the Vector Timer circuit. $\overline{\text{STOP}}$ is set low when Vector Timers N6, M6, P6, and R6 have reached their maximum count. If $\overline{\text{STOP}}$ is low, $\overline{\text{VCTR}}$ from Vector Flag latch E5 and $\overline{\text{CNTR}}$ from Center Flag latch E5 are both set low when E5 is clocked by the 12-MHz clock signal.

$\overline{\text{STROBE0}}$

Strobe 0 is an active low-level signal software-generated by State Machine decoder H7. $\overline{\text{STROBE0}}$ is the clock signal for Normalization Flag latch A6. It is also the $\overline{\text{STROBE0}}$ input for Vector Address Controller J9.

$\overline{\text{STROBE1}}$

Strobe 1 is an active low-level signal software-generated by State Machine decoder H7. If OP2 is low, when $\overline{\text{STROBE1}}$ goes low, the data latched at the outputs of D7 in the Vector Scaling circuit are loaded into counter C7. When $\overline{\text{STROBE1}}$ goes high, C7 begins counting down.

$\overline{\text{STROBE1}}$ is the $\overline{\text{STROBE1}}$ input for Vector Address Controller J9.

$\overline{\text{STROBE2}}$

Strobe 2 is an active low-level signal software-generated by State Machine decoder H7. If OP2 and $\overline{\text{DVY12}}$ are both low, $\overline{\text{SCALELD}}$ from gate J6 is set low when $\overline{\text{STROBE2}}$ goes low. If OP2 and DVY12 are both low, $\overline{\text{STATCLK}}$ is set low when $\overline{\text{STROBE2}}$ goes low.

$\overline{\text{STROBE2}}$ is the $\overline{\text{STROBE2}}$ input for Vector Address Controller J9.

$\overline{\text{STROBE3}}$

Strobe 3 is an active low-level signal software-generated by State Machine decoder H7. $\overline{\text{STROBE3}}$ is the clock signal for Halt Flag latch L5 and is the $\overline{\text{STROBE3}}$ input for Vector Address Controller J9.

If OP0, OP2, $\overline{\text{OP2}}$, and VGCK are all low, VCTR from Vector Flag latch E5 and $\overline{\text{CNTR}}$ from Center Flag latch E5 are both set high when $\overline{\text{STROBE3}}$ goes low.

ST0-ST2

State signals ST0-ST2 are active high-level signals that are software-generated by State Machine ROM N4. These signals, together with ST3, are decoded by H7 of the State Machine circuit to produce LATCH0-LATCH3 and $\overline{\text{STROBE0}}$-$\overline{\text{STROBE3}}$. ST2 is used to develop ST3 and is also the ST2 input for Vector Address Controller J9.

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Gravitar™ PCB Signal Name Descriptions

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SP-206 Sheet 10A
1st printing

Description of Gravitar PCB Signal Names (continued)

ST3

State signal ST3 is an active high-level signal hardware-generated by Decoder Disable latch A7. ST3 is opposite in state to VGCK, and is delayed by one pulse of the 12-MHz clock signal if the Q4 output from State Machine ROM N4 is low and $\overline{VMEM}$ is high. If the Q4 output from N4 is high, ST3 is high. When ST3 is high, State Machine decoder H7 is disabled. When ST3 is low, H7 decodes the data on lines ST0-ST2 to produce $\overline{LATCH0}$-$\overline{LATCH3}$ and $\overline{STROBE0}$-$\overline{STROBE3}$.

VCTR, $\overline{VCTR}$

The Vector Flag signals are software-generated by Vector Flag latch E5. If OP0, OP2, $\overline{STROBE3}$, and VGCK are low and $\overline{HALT}$ is high, VCTR is set high and $\overline{VCTR}$ is set low when E5 is clocked by the 12-MHz clock signal. VCTR is ORed with CNTR by gate M5 to set GO high.

SCALE, CNTR, DVY11-DVY12, and DVX11-DVX12 are gated with VCTR to produce the clear signal for Nomalization Flag latch A6.

In the Z Intensity and Blanking circuit, VCTR is the clock signal for latch H6 and the serial input signal for shift register M3.

VCTR and $\overline{VCTR}$ are used by the DAC Reference and Bipolar Current Sources circuit to set the X BIP, Y BIP, X REF, and Y REF levels.

VGCK

The Vector Generator clock signal is generated at pin 18 of buffer B1 in the Microprocessor circuit. VGCK is derived from the 1.5 MHz clock signal and is applied to AND gate J5 of the State Machine Clock Logic circuit. VGCK is the basic timing signal of the State Machine circuit.

$\overline{VGGO}$

The Vector Generator Go signal is an active low-level signal software-generated by Address Decoder P3 at address 8840. $\overline{VGGO}$ is the clear signal for latch L5 of the Halt Flag circuit. When low, $\overline{VGGO}$ sets HALT to the inactive low level.

$\overline{VGRST}$

Vector Generator Reset is an active low-level signal software-generated by Address Decoder P3 at address 8880. $\overline{VGRST}$ is ORed with $\overline{RESET}$ by gate L6 of the Halt Flag circuit to produce $\overline{DISRST}$.

$\overline{VMEM}$

The Vector Memory Select Enable is an active low-level signal software-generated by Address Decoder R1 during addresses 2000 through 5FFF. $\overline{VMEM}$ is the select-enable signal for Vector Address Selectors K8, L8, M8, and N8. When low, $\overline{VMEM}$ allows the Vector Address Selectors to produce $\overline{VW}$, $\overline{BUFFEN}$, and the AM0-AM12 multiplexed address bits. $\overline{VMEM}$ is also applied to gate K5 of the State Machine Clock Logic circuit where it is used to generate ST3.

$\overline{VRAM}$

The Vector Random-Access Memory Chip Enable is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2000-27FF. When low, $\overline{VRAM}$ enables Vector Random-Access Memory K7 to be addressed to either receive or transmit data, depending upon the state of $\overline{VW}$. $\overline{VRAM}$ is also used to produce the SAEN signal from M5 of the Vector Address Selector circuit.

$\overline{VROM0}$

Vector Read-Only Memory Chip Select 0 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 2800-2FFF. $\overline{VROM0}$ is the chip-select signal for ROM L7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM0}$ allows ROM L7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VROM1}$

Vector Read-Only Memory Chip Select 1 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 3000-3FFF. $\overline{VROM1}$ is the chip-select signal for ROM M/N7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM1}$ allows ROM M/N7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VROM2}$

Vector Read-Only Memory Chip Select 2 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 4000-4FFF. $\overline{VROM2}$ is the chip-select signal for ROM N/P7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM2}$ allows ROM N/P7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VROM3}$

Vector Read-Only Memory Chip Select 3 is an active low-level signal software-generated by Vector Address Decoder J7 at addresses 5000-5FFF. $\overline{VROM3}$ is the chip-select signal for ROM R7 of the Vector Read-Only Memory circuit. When low, $\overline{VROM3}$ allows ROM R7 to be addressed and to pass data to the Vector Generator Data Bus.

$\overline{VW}$

The Vector Write Enable is an active low-level signal software-generated from Vector Address Selector K8, ANDed with $\overline{B\Phi 2}$ by gate J6, and applied as the write-enable signal for Vector Random-Access Memory K7. When low, $\overline{VW}$ allows data to be written to K7; when high, $\overline{VW}$ permits data to be read from K7.

$\overline{WDCLR}$

Watchdog Clear is an active low-level signal software-generated by Address Decoder P3 at address 8980. $\overline{WDCLR}$ is ORed with $\overline{POR}$ by gate E3 to clear the count of Watchdog counter H4.

$\overline{WDDIS}$

Watchdog Disable is a test point at pin 9 of AND gate L4 in the Watchdog circuit. When $\overline{WDDIS}$ is grounded, $\overline{RESET}$ is prevented from going to an active low level (except when the RESET test point is grounded).

$\overline{WRITE}$

Write Enable is an active low-level signal generated by gate K4 of the Microprocessor circuit. $\overline{WRITE}$ is used to enable Address Decoder P3 and Random-Access Memory N/P1. $\overline{WRITE}$ is also applied to pin 11 of K8 in the Vector Address Selector circuit to develop $\overline{VW}$.

X BIP

The X-Axis Bipolar Current is set by R99 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

X OUT

X Output is a game PCB output signal generated by the X-Axis Output circuit. X OUT carries the horizontal beam deflection signal for the drawing of vectors on the display.

X REF

The X-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of X-axis digital-to-analog converter (DAC) A/B9 of the X-Axis Output circuit.

Y BIP

The Y-Axis Bipolar Current is set by R98 of the DAC Reference and Bipolar Current Sources circuit. This is the current source for pin 18 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Y OUT

Y Output is a game PCB output signal generated by the Y-Axis Output circuit. Y OUT carries the vertical beam deflection signal for the drawing of vectors on the display.

Y REF

The Y-Axis Voltage Reference is set by the DAC Reference and Bipolar Current Sources circuit. This is the reference voltage applied to pin 14 of Y-axis digital-to-analog converter (DAC) F9 of the Y-Axis Output circuit.

Z0-Z2, $\overline{Z1}$-$\overline{Z2}$

Z Intensity signals Z0-Z2 and $\overline{Z1}$-$\overline{Z2}$ are software-generated by latch C6 in the Op Code and Intensity Latches circuit. These signals are derived from the data on lines DVG51-DVG7 when C6 is clocked by $\overline{LATCH3}$. If the binary count carried by Z0-Z2 is not equal to 1, these signals are the input signals for latch F6 in the Z Intensity and Blanking circuit. If the binary count carried by Z0-Z2 is 1, Z Intensity signals Z0, $\overline{Z1}$, and $\overline{Z2}$ are ANDed by gate F5 of the Z Intensity and Blanking circuit to produce the select signal for latch F6. This select signal causes the latched data from E6 to be applied as the input signals for latch F6.

Z OUT

Z Intensity Output is a game PCB output signal generated by the Z Intensity and Blanking circuit from either DVY4-DVY7 or Z0-Z2. The Q output signals from latch H6 are summed at the base of Q7. Transistors Q7 and Q9 buffer Z OUT before it is sent to the game display circuitry to control the display intensity.

3 KHZ

The 3 kHz clock signal is generated at pin 6 of Clock counter F4 and is applied through switch input buffer M9 of the Coin Door and Control Panel Input circuit (when $\overline{SINP1}$ is low). The 3 kHz clock is read by the microprocessor on data line DB7. This frequency is the time reference for the Microprocessor C2.

12 KHZ

The 12 kHz clock signal is generated at pin 4 of Clock counter F4 and is applied to reset A4 of the High-Score Table.

3 MHZ

The 3 MHz clock signal is generated at pin 2 of Clock counter F4. The 3 MHz signal is ANDed with R/$\overline{WB}$ and BΦ2 by gate K4 to produce $\overline{WRITE}$. It is also applied to AND gate J5 of the State Machine Clock Logic and to shift register M3 of the Z Intensity and Blanking circuit.

6 MHZ

The 6 MHz clock signal is generated at pin 3 of Clock counter F4 and is applied to gate J5 of the State Machine Clock Logic circuit.

12 MHZ

The 12 MHz clock signal is generated at pin 10 of inverter F3 in the Clock circuit. This signal clocks the Vector Timer Shifters, the Vector Flag latch, and the Center Flag latch.

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Gravitar™ PCB Signal Name Descriptions

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SP-206 Sheet 10B
1st printing

Troubleshooting with the Read/Write Controller

A. CAT Box Preliminary Set-Up

1. Remove the electrical power from the game.
2. Remove the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet.
4. Remove Microprocessor C2 from the game PCB.
5. Connect the harness from the game to the game PCB. (Use extender cables, if available.)
6. Connect together the Φ0 and Φ2 test points on the game PCB with the shortest possible jumper.
7. Connect the $\overline{\text{WDDIS}}$ test point to ground.
8. Connect the CAT Box flex cable to the game PCB edge test connector.
9. Apply power to the game and to the CAT Box.
10. Set CAT Box switches as indicated:
    a. TESTER SELF-TEST: OFF
    b. TESTER MODE: R/$\overline{W}$
11. Press TESTER RESET.

B. Address Lines

1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box.
3. Connect the DATA PROBE ground clip to a game PCB ground test point.
4. Set CAT Box switches as indicated:
    a. BYTES: 1
    b. PULSE MODE: UNLATCHED
    c. R/$\overline{W}$ MODE: (OFF)
    d. R/$\overline{W}$: WRITE
5. Key in the address pattern given in Table 1 *(use AAAA to start)* with the CAT Box keyboard.
6. Press DATA SET.
7. Key in the data pattern given in Table 1 *(use AA to start)* with the keyboard.
8. Set R/$\overline{W}$ MODE: STATIC
9. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 1 lights up. Repeat this step for each address line listed in Table 1.
10. Repeat parts 4-c through 9 using address *5555* in part 5 and data *55* in part 7.

C. Data Lines

1. Perform the CAT Box preliminary set-up.
2. Connect the DATA PROBE to the CAT Box.

Table 1 Address Lines

When writing *AAAA* pattern	Address lines	When writing *5555* pattern
LOGIC STATE	**IC-PIN**	**LOGIC STATE**
1	R2-12	0
0	R2-13	1
1	R2-14	0
0	B1-5	1
1	B1-7	0
0	B1-12	1
1	B1-14	0
0	B1-16	1
1	C1-9	0
0	C1-7	1
1	C1-5	0
0	C1-3	1
1	C1-12	0
0	C1-14	1
1	C1-16	0
0	C1-18	1

3. Connect the DATA PROBE ground clip to the game PCB ground test point.
4. Set CAT Box switches as indicated:
    a. BYTES:1
    b. R/$\overline{W}$ MODE: (OFF)
    c. R/$\overline{W}$: WRITE
5. Key in address *0000* with the keyboard.
6. Press DATA SET.
7. Key in data *AA* with the keyboard.
8. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
9. Probe the IC-pin with the DATA PROBE and check that the 1 or 0 LED indicated in Table 2 lights up. Repeat this check for each IC-pin in Table 2.
10. Repeat parts 6 through 9 using data *55* in part 7.

D. RAM

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
    a. DBUS SOURCE: ADDR
    b. BYTES:1024
    c. R/$\overline{W}$ MODE: (OFF)
    d. R/$\overline{W}$: WRITE
3. Enter address *0000* with the keyboard.
4. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
5. Set R/$\overline{W}$: READ.
6. Set R/$\overline{W}$ MODE to PULSE and back to (OFF).
7. If the CAT Box reads an address that doesn't compare with that written, the COMPARE ERROR LED will light up. The ADDRESS/SIGNATURE display of the CAT Box will show the failing address location and the ERROR DATA DISPLAY switch is enabl-

MEMORY MAP

HEXA-DECIMAL ADDRESS	ADDRESS BUS A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R/W	DATA BUS D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
E000-EFFF	1	1	1		A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 5}}$
D000-DFFF	1	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 4}}$
C000-CFFF	1	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 3}}$
B000-BFFF	1	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 2}}$
A000-AFFF	1	0	1	0	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 1}}$
9000-9FFF	1	0	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{ROM 0}}$
8800	1	0	0	0	1												R	D								CABINET 1
																			D							$\overline{\text{START 2}}$
																				D						$\overline{\text{START 1}}$
																					D					$\overline{\text{THRUST 2}}$
																						D				$\overline{\text{ROT LEFT 2}}$
																							D			$\overline{\text{ROT RIGHT 2}}$
																								D		$\overline{\text{FIRE 2}}$
																									D	$\overline{\text{SHIELDS 2}}$
89C0	1	0	0	0	1	0	0	1	1	1							W									$\overline{\text{SPARE WT}}$
8980	1	0	0	0	1	0	0	1	1	0							W									$\overline{\text{WDCLR}}$
8940	1	0	0	0	1	0	0	1	0	1	D	D	D	D	D	D	W	D	D	D	D	D	D	D	D	$\overline{\text{EAROMWR}}$
8900	1	0	0	0	1	0	0	1	0	0							W					D	D	D	D	$\overline{\text{EAROMCON}}$
88C0	1	0	0	0	1	0	0	0	1	1							W									$\overline{\text{INTACK}}$
8880	1	0	0	0	1	0	0	0	1	0							W									$\overline{\text{VGRST}}$
8840	1	0	0	0	1	0	0	0	0	1							W									$\overline{\text{VGGO}}$
8800	1	0	0	0	1	0	0	0	0	0							W	D								INVERT Y
																			D							INVERT X
																				D						$\overline{\text{PLAYER 2 LED}}$
																					D					PLAYER 1 LED
																						D				COIN LOCKOUT
																							D			BANK SEL
																								D		COIN CNTR-L
																									D	COIN CNTR-R
8000	1	0	0	0	0												R	D								OPTION 2
																			D							OPTION 1
																				D						OPTION 0
																					D					$\overline{\text{THRUST 1}}$
																						D				$\overline{\text{ROT LEFT 1}}$
																							D			$\overline{\text{ROT RIGHT 1}}$
																								D		$\overline{\text{FIRE 1}}$
																									D	$\overline{\text{SHIELDS 1}}$
7800	0	1	1	1	1												R	D								3 KHZ
																			D							HALT
																				D						$\overline{\text{SA}}$
																					D					SELF-TEST
																						D				$\overline{\text{COIN-AUX}}$
																							D			$\overline{\text{COIN L}}$
																								D		$\overline{\text{COIN R}}$
7000	0	1	1	1	0												R	D	D	D	D	D	D	D	D	$\overline{\text{EAROMRD}}$
6800	0	1	1	0	1												R/$\overline{W}$	D	D	D	D	D	D	D	D	$\overline{\text{I/O0}}$
6000	0	1	1	0	0												R/$\overline{W}$	D	D	D	D	D	D	D	D	$\overline{\text{I/O1}}$
5000-5FFF	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 3}}$
4000-4FFF	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 2}}$
3000-3FFF	0	0	1	1	A	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 1}}$
2800-2FFF	0	0	1	0	1	A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	$\overline{\text{VROM 0}}$
2000-27FF	0	0	1	0	0	A	A	A	A	A	A	A	A	A	A	A	R/$\overline{W}$	D	D	D	D	D	D	D	D	$\overline{\text{VRAM}}$
0000-07FF	0	0	0	0	0	A	A	A	A	A	A	A	A	A	A	A	R/$\overline{W}$	D	D	D	D	D	D	D	D	$\overline{\text{RAM}}$

ATARI®

Gravitar™ PCB Troubleshooting

SP-206 Sheet 11A
1st printing

ed. Using this switch, determine if the error is in the high-order or low-order RAM.

8. Repeat parts 2-d through 7 using addresses *0400, 2000,* and *2400* .
9. Repeat this test with DBUS SOURCE set to $\overline{\text{ADDR}}$.

E. Custom Audio I/O Chips

NOTE

Gravitar has two custom audio I/O chips. Each must be tested separately. There are several ways to test these chips:

- Perform the self-test.
- Substitute a known good part for a suspected defective part.
- Use the following procedure.

1. Perform the CAT Box preliminary set-up.

Table 2 Data Lines

When writing *AA* pattern	Data lines	When writing *55* pattern
LOGIC STATE	IC-PIN	LOGIC STATE
1	F2-11	0
0	F2-12	1
1	F2-13	0
0	F2-14	1
1	F2-15	0
0	F2-16	1
1	F2-17	0
0	F2-18	1
1	F2-9	0
0	F2-8	1
1	F2-7	0
0	F2-6	1
1	F2-5	0
0	F2-4	1
1	F2-3	0
0	F2-2	1

2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{\text{W}}$: WRITE
   c. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter the address from Table 3 with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 3 with the keyboard.
6. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
7. Repeat parts 3 through 6 for each address and data listed in Table 3. Check for the response indicated.

Table 3 Custom Audio I/O Chips

ADDRESS	DATA	TEST RESULTS
680F	*00*	
680F	*03*	
6800	*55*	
6801	*AF*	Custom Audio I/O Chip B3 channel 1 produces pure tone.
6801	*00*	Custom Audio I/O Chip B3 channel 1 off.
6802	*55*	
6803	*AF*	Custom Audio I/O Chip B3 channel 2 produces pure tone.
6803	*00*	Custom Audio I/O Chip B3 channel 2 off.
600F	*00*	
600F	*03*	
6000	*55*	
6001	*AF*	Custom Audio I/O Chip C/D3 channel 1 produces pure tone.
6001	*00*	Custom Audio I/O Chip C/D3 channel 1 off.
6002	*55*	
6003	*AF*	Custom Audio I/O Chip C/D3 channel 2 produces pure tone.
6003	*00*	Custom Audio I/O Chip C/D3 channel 2 off.

F. Player and Option Switch Inputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. BYTES: 1
   b. R/$\overline{\text{W}}$: READ
3. For each address listed in Table 4, do the following:
   a. Set R/$\overline{\text{W}}$ MODE to (OFF).
   b. Enter the address with the keyboard.
   c. Set R/$\overline{\text{W}}$ MODE to STATIC.
   d. Activate the input switch indicated in Table 4 for the address.

Table 4 Player and DIP Switch Inputs

ADDRESS	INPUT SWITCH	TEST RESULTS
7800	Right coin switch Left coin switch Self-test switch	Lower nybble (right digit) of DATA display changes when right or left coin, or self-test switches are activated. Upper nybble of DATA display is unstable.
8000	Player 1 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START	Upper nybble of DATA display changes when each input switch is activated.
8800	Player 2 SHIELDS, FIRE, ROTATE LEFT, ROTATE RIGHT, THRUST, START	Upper nybble of DATA display changes when each input switch is activated.

G. Analog Vector-Generator

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. R/$\overline{\text{W}}$: WRITE
   c. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter address *2000* with the keyboard.
4. Press DATA SET.
5. Enter the data from Table 5.
6. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
7. Repeat parts 4 through 6 for each address listed in Table 5 using the ADDRESS INCR button to advance the address by 1.

CAUTION

You may damage the circuitry of the X-Y display if you key in the $\overline{\text{VGGO}}$ signal without first checking all the addresses and data. Check the data by reading each address location using parts 8 though 11 below.

8. Set CAT Box switches as indicated:
   a. R/$\overline{\text{W}}$: READ
   b. R/$\overline{\text{W}}$ MODE: (OFF)
9. Enter address or press ADDRESS INCR.
10. Set R/$\overline{\text{W}}$ MODE to PULSE.
11. Check the data shown in the DATA display against that listed in Table 5. If the data is correct, proceed with part 12.
12. Set CAT Box switches as indicated:
    a. R/$\overline{\text{W}}$: WRITE
    b. R/$\overline{\text{W}}$ MODE: (OFF)

ATARI®

Gravitar™ PCB Troubleshooting

A Warner Communications Company

SP-206 Sheet 11B
1st printing

13. Enter $\overline{\text{VGGO}}$ address *8840* .
14. Set R/$\overline{\text{W}}$ MODE to PULSE and back to (OFF).
15. Check that the screen shows a large plus sign. Failure of the horizontal or vertical circuits shows up as a single line drawn on the screen. *If the screen does not display a large plus sign, contact Atari Field Service.*

Table 5 Analog Vector-Generator Data

ADDRESS	DATA	ADDRESS	DATA
2000	*00*	*200C*	*00*
2001	*70*	*200D*	*21*
2002	*40*	*200E*	*80*
2003	*80*	*200F*	*1F*
2004	*77*	*2010*	*80*
2005	*64*	*2011*	*1F*
2006	*00*	*2012*	*00*
2007	*00*	*2013*	*01*
2008	*80*	*2014*	*00*
2009	*1F*	*2015*	*20*
200A	*00*	*2016*	*00*
200B	*00*	*2017*	*E0*

H. LED, Coin Counter, and Invert Outputs

1. Perform the CAT Box preliminary set-up.
2. Set CAT Box switches as indicated:
   a. DBUS SOURCE: DATA
   b. BYTES: 1
   c. R/$\overline{\text{W}}$: WRITE
   d. R/$\overline{\text{W}}$ MODE: (OFF)
3. Enter address *8800* with the keyboard.

CAUTION

If you write ON data to activate a solenoid, *deactive the solenoid immediately* by writing the OFF data. If you leave a solenoid activated for more than 10 seconds, you may have to replace the solenoid and/or its driver, due to overheating.

4. For each DATA output listed in Table 5, do the following:
   a. To activate the output:
      - Press DATA SET.
      - Enter the ON data listed for the output.
      - Set R/$\overline{\text{W}}$ MODE to STATIC and back to (OFF).
   b. To deactivate the output:
      - Press DATA SET.
      - Enter the OFF data listed for the output.
      - Set R/$\overline{\text{W}}$ MODE to STATIC and back to (OFF).

Table 6 LED and Coin Counter Outputs

ON DATA	OFF DATA	OUTPUT DEVICE
00	*10*	Player 1 LED
00	*20*	Player 2 LED
01	*00*	Right Coin Counter
02	*00*	Left Coin Counter
08	*00*	Coin Door Lockout
40	*00*	INVERT X*
80	*00*	INVERT Y**

*When INVERT X is activated, check for logic 1 on pin 16 of IC B10.

**When INVERT Y is activated, check for logic 1 on pin 16 of IC E10.

Troubleshooting with Signature Analysis

A. Signature Analysis Set-Up

1. Perform the CAT Box preliminary set-up.
2. Connect the three BNC-to-EZ clip cables supplied with CAT Box to the SIGNATURE ANALYSIS CONTROL START, STOP, and CLOCK jacks of the CAT Box.
3. Connect the three black EZ clips to a game PCB ground test point.
4. Connect the CAT Box DATA PROBE to the DATA jack on the CAT Box.
5. Set the CAT Box switches as indicated:
   a. TESTER MODE: SIG
   b. TESTER SELF-TEST: OFF
   c. PULSE MODE: LATCHED
   d. START: Negative-going edge trigger
   e. STOP: Negative-going edge trigger
   f. CLOCK: Negative-going edge trigger

B. Address Lines

1. Perform the signature analysis set-up.
2. Connect the START probe tip to pin 14 of IC R2.
3. Connect the STOP probe tip to pin 14 of IC R2.
4. Connect the CLOCK probe tip to Φ2 test point on the game PCB.
5. Verify the set-up connections by connecting the DATA PROBE to a game PCB ground test point. The CAT Box ADDRESS/SIGNATURE display should show *0000*. Now connect the DATA PROBE to a +5V test point; the ADDRESS/SIGNATURE display should show *0001*.
6. Probe the IC-pin listed in Table 7 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 7 Address Bus Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
C1-18	AB0	*UUUU*
C1-16	AB1	*5555*
C1-14	AB2	*CCCC*
C1-12	AB3	*7F7F*
C1-3	AB4	*5H21*
C1-5	AB5	*0AFA*
C1-7	AB6	*UPFH*
C1-9	AB7	*52F8*
B1-16	AB8	*HC89*
B1-14	AB9	*2H70*
B1-12	AB10	*HPP0*
B1-7	AB11	*1293*
B1-5	AB12	*HAP7*
R2-12	A13	*3C96*
R2-13	A14	*3827*
R2-14	A15	*755U*

C. Address Decoder

CAUTION

While testing decoders and ROMs, adding 270 pF capacitors to AB12, A13, A14, and A15 may be necessary to eliminate unstable signatures.

1. Perform parts 1 through 5 of the address bus signature procedure.
2. Probe the IC-pin listed in Table 8 with the DATA PROBE and check for the signature indicated. Repeat this check for each IC-pin listed.

Table 8 Decoder Signatures

IC-PIN	SIGNAL NAME	SIGNATURE
R2-1	$\overline{\text{RAM}}$	*3APF*
R2-2	$\overline{\text{I/O0}}$	*85H4*
R2-3	$\overline{\text{I/O1}}$	*131H*
R2-4	$\overline{\text{I/OS}}$	*96F9*
R2-5	$\overline{\text{EAROMRD}}$	*F042*
R2-6	$\overline{\text{SINP1}}$	*942F*
R2-7	$\overline{\text{SINP2}}$	*3PCF*
R2-9	$\overline{\text{IO}}$	*84AF*
R1-1	$\overline{\text{VMEM}}$	*U9U3*
R1-2	ROM	*FU4U*
R1-3	$\overline{\text{ROM0}}$	*H759*
R1-4	$\overline{\text{ROM1}}$	*A3UH*
R1-5	$\overline{\text{ROM2}}$	*AA6A*
R1-6	$\overline{\text{ROM3}}$	*A711*
R1-7	$\overline{\text{ROM4}}$	*54F5*
R1-9	$\overline{\text{ROM5}}$	*P255*

Watchdog Troubleshooting

The Watchdog circuit will send continuous reset pulses to the microprocessor if a problem exists within the microprocessor circuit. If the self-test fails to run, it is a good practice to check the reset line.

RESET is a microprocessor input (pin 40). In a properly operating game, reset should occur during power-up or when the RESET test point is grounded. A pulsing $\overline{\text{RESET}}$ line indicates that something is causing the microprocessor to lose its place within the program. Typical causes are:

1. Open or shorted address or data bus lines.
2. Bad microprocessor chip.
3. Bad bus buffers.
4. Bad ROM.
5. Bad RAM.
6. Any bad input or output that causes an address or data line to be held in a constant high or low state.

A pulsing $\overline{\text{RESET}}$ signal indicates a problem exists somewhere within the microprocessor circuitry rather than within the analog vector-generator.

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Gravitar™ PCB Troubleshooting

SP-206 Sheet 12A
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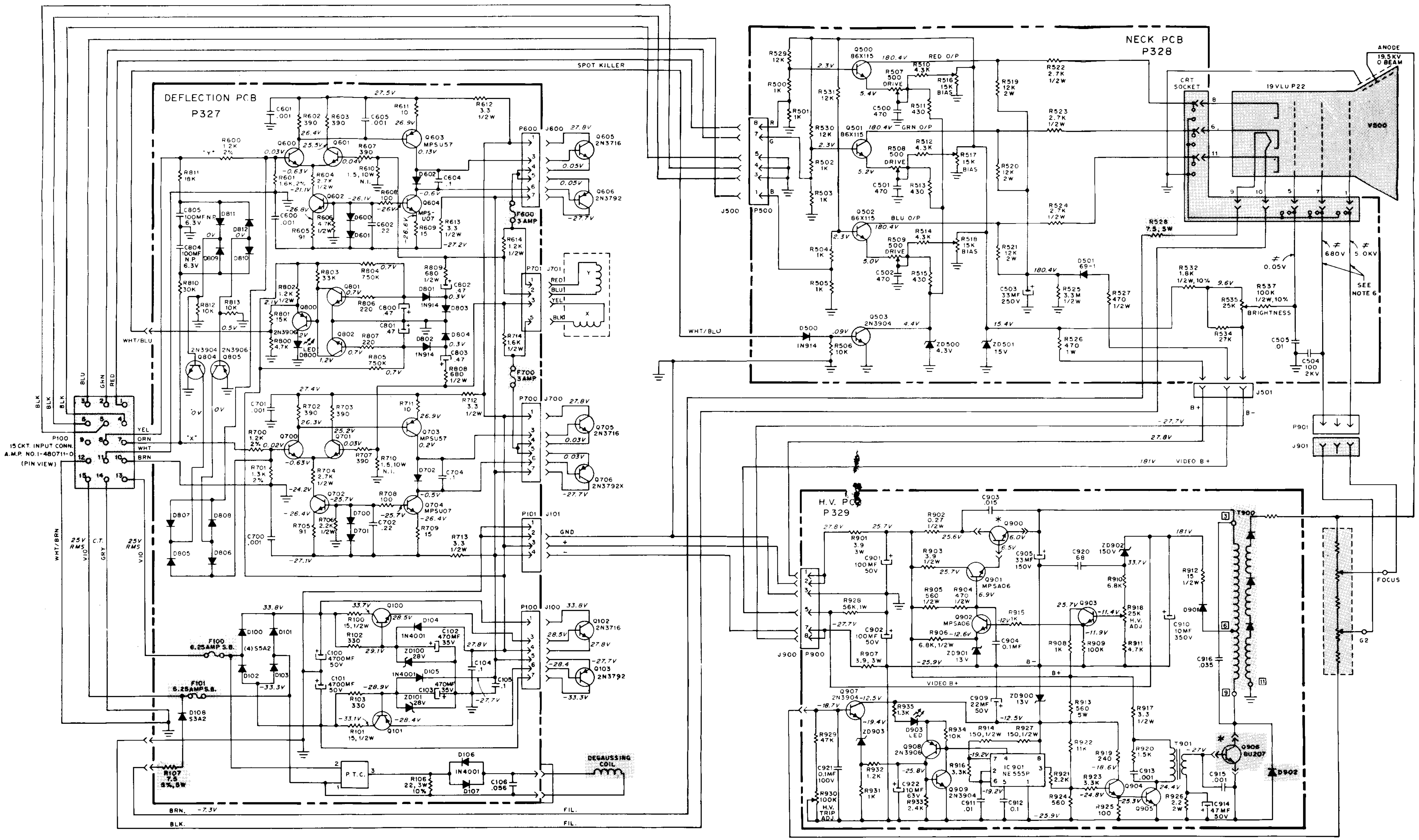

WARNING

Components identified by shading have special characteristics important to safety and should be replaced only with identical types.

GENERAL NOTES

1. Resistance values in ohms, ¼ watt, ±5%, unless otherwise noted. K = 1,000, M = 1,000,000
2. Capacitance value of 1 or less is in microFarads, above 1 in picoFarads, unless otherwise noted.
3. * Q900 and Q906 are not in High-Voltage PCB.
4. All D.C. voltages are ±10% measured from point indicated to ground, using a high-impedance meter. Voltages are measured with no signal input and controls are in a normal operating position.
5. Circled numbers indicate location of waveform reading.
6. ZD100-101 uses (66X0040-007) zener diode in series with (340X2331-934) 330-ohm resistor in early production models.
7. Use a 1,000:1 probe when measuring G2 (screen) or focus voltage.

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Wells Gardner
Color X-Y Display Schematic Diagram

SP-206 Sheet 12B
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