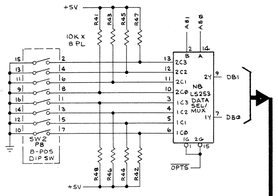
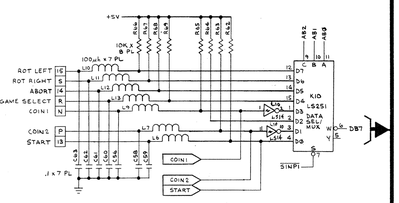
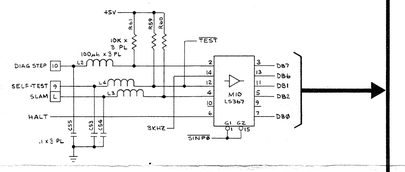
OPTIONS INPUT CIRCUITRY



The game option switches are read by the MPU when OPTS (option switch enable) is low. Switch toggles to be read are selected by AB0 and AB1 from the MPU. Switch toggles 1, 3, 6, and 7 are read on data line DB0 and toggles 2, 4, 6 and 8 are read on DBI. Toggle inputs are "on" when pulled to ground.

SWITCH INPUT



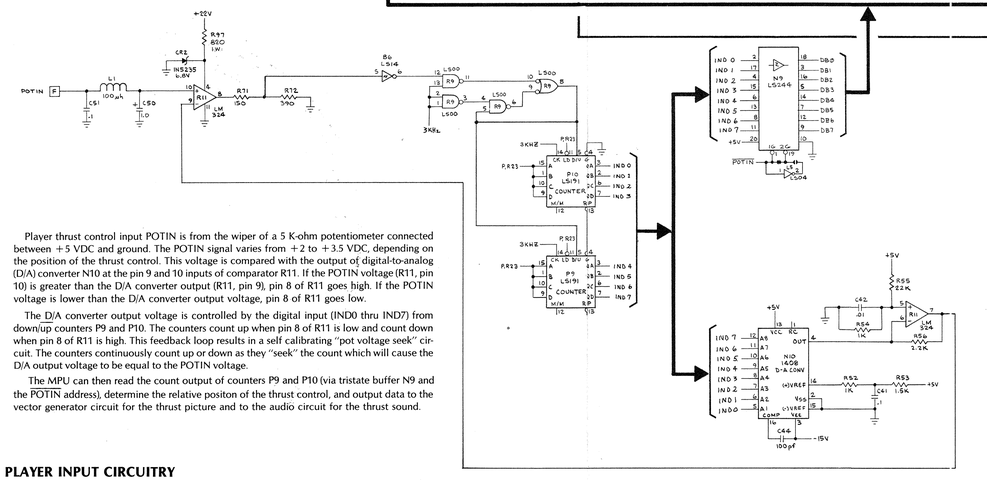


NOTE:
= TEST POINT

The coin door and control panel switches are read by the MPU when SINP1 (switch input one enable) is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

DIAG STEP (diagnostic step), 3 KHz, SELF-TEST, SLAM, and HALT inputs are read by the MPU when SINP0 (switch input zero enable) is low. Inputs are directly read by the MPU on data lines DB7, DB6, DB1, DB2, and DB0 respectively. Switch inputs are active when pulled to ground. DIAG. STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antislam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

THRUST INPUT



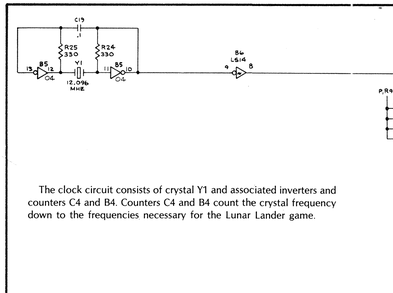
Player thrust control input POTIN is from the wiper of a 5 K-ohm potentiometer connected between +5 VDC and ground. The POTIN signal varies from +2 to +3.5 VDC, depending on the position of the thrust control. This voltage is compared with the output of digital-to-analog (D/A) converter N10 at the pin 9 and 10 inputs of comparator R11. If the POTIN voltage (R11, pin 10) is greater than the D/A converter output (R11, pin 9), pin 8 of R11 goes high. If the POTIN voltage is lower than the D/A converter output voltage, pin 8 of R11 goes low.

The D/A converter output voltage is controlled by the digital input (IND0 thru IND7) from down/up counters P9 and P10. The counters count up when pin 8 of R11 is low and count down when pin 8 of R11 is high. This feedback loop results in a self calibrating "pot voltage seek" circuit. The counters continuously count up or down as they "seek" the count which will cause the D/A output voltage to be equal to the POTIN voltage.

The MPU can then read the count output of counters P9 and P10 (via tristate buffer N9 and the POTIN address), determine the relative positon of the thrust control, and output data to the vector generator circuit for the thrust picture and to the audio circuit for the thrust sound.

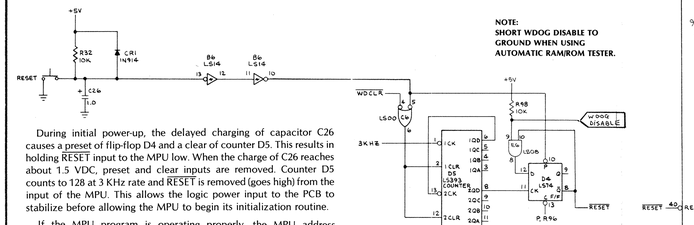
PLAYER INPUT CIRCUITRY

MPU CIRCUITRY



The clock circuit consists of crystal Y1 and associated inverters and counters C4 and B4. Counters C4 and B4 count the crystal frequency down to the frequencies necessary for the Lunar Lander game.

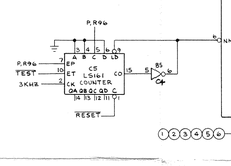
CLOCK CIRCUIT



During initial power-up, the delayed charging of capacitor C26 causes a preset of flip-flop D4 and a clear of counter D5. This results in holding RESET input to the MPU low. When the charge of C26 reaches about 1.5 VDC, preset and clear inputs are removed. Counter D5 counts to 128 at 3 KHz rate and RESET is removed (goes high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

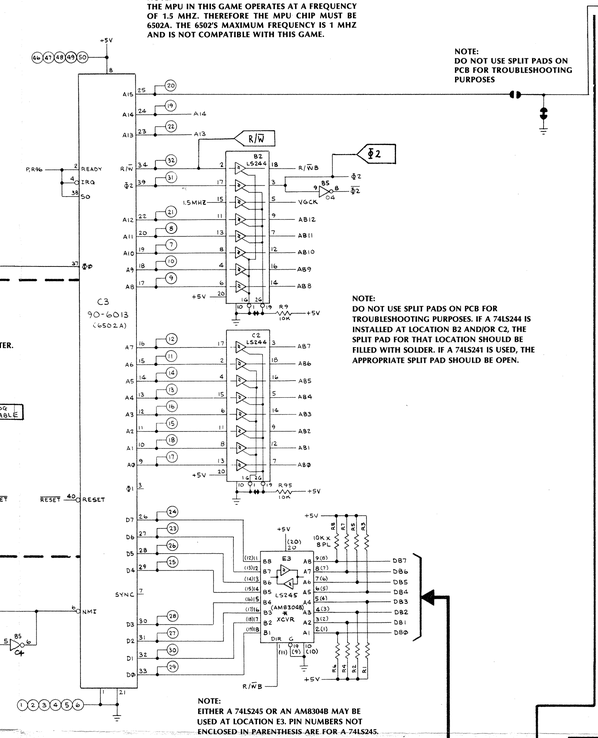
If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCLR (Watchdog clear) signal at predetermined intervals. This serves to clear counter D5 before it counts up to the state that will create the RESET condition. If the MPU program strays from its intended sequence and does not output the WDCLR signal, counter D5 will count up to the RESET state and cause the MPU to return to its initialization routine.

POWER RESET AND WATCHDOG COUNTER



The NMI (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 msec. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 6 of inverter B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

NMI COUNTER



NOTE:
THE MPU IN THIS GAME OPERATES AT A FREQUENCY OF 1.5 MHZ. THEREFORE THE MPU CHIP MUST BE 6502A. THE 6502'S MAXIMUM FREQUENCY IS 1 MHZ AND IS NOT COMPATIBLE WITH THIS GAME.

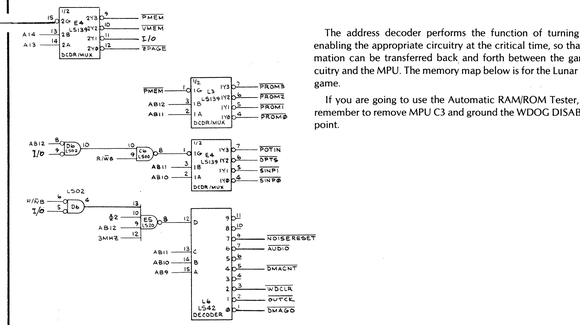
NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES

NOTE:
SHORT WDOG DISABLE TO GROUND WHEN USING AUTOMATIC RAM/ROM TESTER.

NOTE:
DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES. IF A 74LS244 IS INSTALLED AT LOCATION B2 AND/OR C2, THE SPLIT PAD FOR THAT LOCATION SHOULD BE FILLED WITH SOLDER. IF A 74LS241 IS USED, THE APPROPRIATE SPLIT PAD SHOULD BE OPEN.

NOTE:
EITHER A 74LS245 OR AN AM8304B MAY BE USED AT LOCATION E3. PIN NUMBERS NOT ENCLOSED IN PARENTHESIS ARE FOR A 74LS245. PIN NUMBERS IN PARENTHESIS ARE FOR AN AM8304B.

ADDRESS DECODING CIRCUITRY



The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Lunar Lander game.

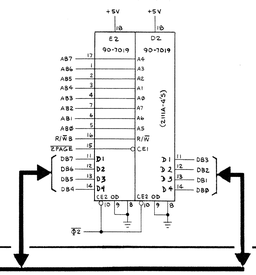
If you are going to use the Automatic RAM/ROM Tester, please remember to remove MPU C3 and ground the WDOG DISABLE test point.

MEMORY MAP

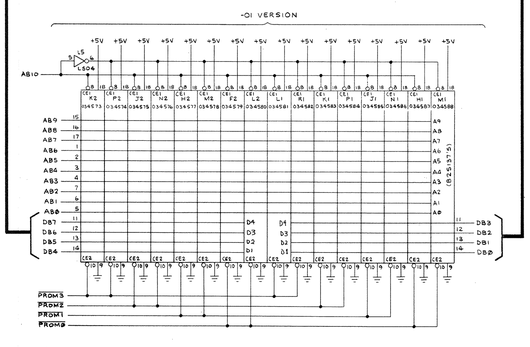
ADDRESS HEXADECIMAL	ADDRESS A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	R/W	DATA D7 D6 D5 D4 D3 D2 D1 D0	FUNCTION
0000-00FF	0 0 A A A A A A A A	R	D D D D D D D D	PAGE ZERO RAM
2000	0 1 0 0 0 0	R	D	HALT
	0 1 0 0 0	R	D	TEST SW
	0 1 0 0 0	R		SLAM SW
	0 1 0 0 0	R	D	3 KHz
2400	0 1 0 0 1 0 0 0	R	D	DIAG STEP
	0 1 0 0 1	R	D	START
1	0 1 0 0 1 0 0 1	R	D	COIN 3
2	0 1 0 0 1 0 1 0	R	D	COIN 2
3	0 1 0 0 1 0 1 1	R	D	COIN 1
4	0 1 0 0 1 1 0 0	R	D	GAME SELECT
5	0 1 0 0 1 1 0 1	R	D	ABORT
6	0 1 0 0 1 1 1 0	R	D	ROT RIGHT
7	0 1 0 0 1 1 1 1	R	D	ROT LEFT
2800	0 1 0 1 0 0 0	R	D D	OPTION
	0 1 0 1 0 0	R	D D	OPTION
3000	0 1 0 1 1 0 0 0 0	W	D	DMACO
3200	0 1 1 0 0 0 1	W	D	ATRACT LAMP 0
	0 1 1 0 0 0	W	D	ATRACT LAMP 1
	0 1 1 0 0 0	W	D	ATRACT LAMP 2
	0 1 1 0 0 0	W	D	ATRACT LAMP 3
3400	0 1 1 0 0 1 0	W	D	START & SELECT LEDS
	0 1 1 0 0 1 0	W	D	COIN COUNTER
	0 1 1 0 0 1 0	W	D	WATCHDOG CLEAR
3800	0 1 1 1 0 0 0	W	D	DMACNT
3C00	0 1 1 1 1 1 0	W	D D D D	THRUST INTENSITY
	0 1 1 1 1 1 0	W	D	THRUST PITCH
	0 1 1 1 1 1 0	W	D D	TONE INTENSITY
3E00	0 1 1 1 1 1 1 1	W		NOISE RESET
4000-47FF	1 0 0 0 A A A A A A A A A A A A	R	D D D D D D D D	VECTOR RAM
4800-4FFF	1 0 0 1 A A A A A A A A A A A A	R	D D D D D D D D	VECTOR ROM
5000-5FFF	1 0 1 A A A A A A A A A A A A	R	D D D D D D D D	VECTOR ROM
6000-7FFF	1 1 A A A A A A A A A A A A A A	R	D D D D D D D D	PROGRAM ROM

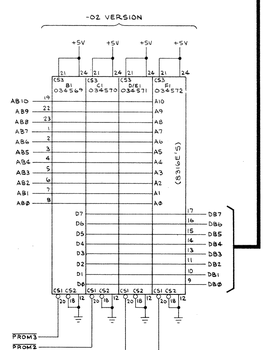
RAM CIRCUITRY

The RAM is the temporary storage space for the MPU and is enabled when ZPAGE (Zero Page enable) is low. When R/WB (from the MPU) is low, the RAM stores the data byte input (DB0 thru DB7) at the location addressed by the MPU address bus (AB0 thru AB7). When R/WB is high, the MPU reads the stored data byte at the addressed location.



ROM/PROM CIRCUITRY





Program Memory for the Lunar Lander game is contained in PROMs for the -01 version of the PCB or ROMs for the -02 version of the PCB. One ROM is equivalent to four PROMs. All PROMs connected to a common enable must be removed before replacing with a ROM. For example, remove PROMs at locations F2, H1, L2 and M1 before replacing with ROM at location F1. A ROM/PROM equivalent chart is contained in Chapter 5, Illustrated Parts Catalog, of the Lunar Lander game manual.

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