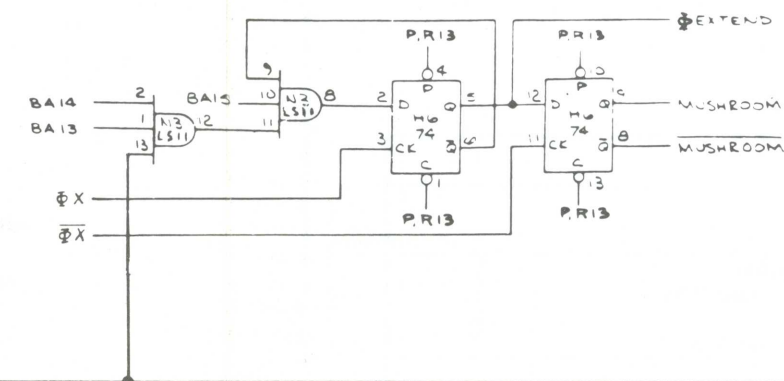


**IRQH (Hardware Interrupt)** - Signal that disables the DRAM Address Controller from putting out a high MADSEL signal.

### 3rd Color Bit Select

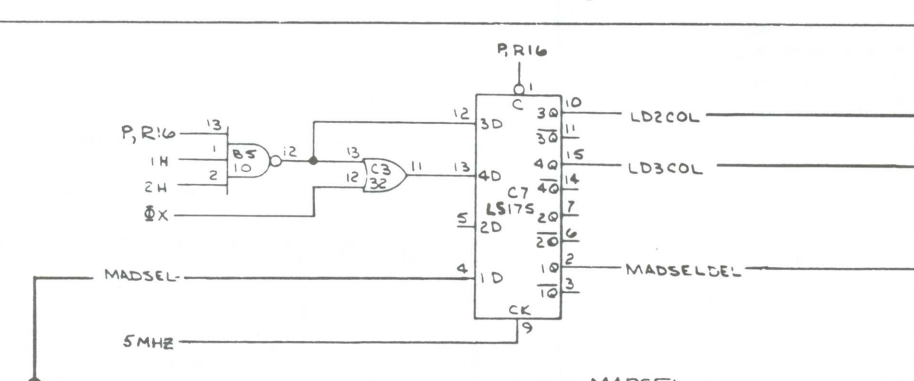


**EXTEND (Clock Extend)** - Microprocessor-generated signal that, when high, delays the  $\Phi 0$  clock input (holds  $\Phi 0$  high) to the microprocessor while the microprocessor accesses the 3rd-color bit region of the DRAM.

**$\Phi X$  (Phase X)** - Sync-generated signal equivalent to 2H (1.25 MHz), except during the last 32 scan lines (cities area) of the video display. At this time  $\Phi X$  pulses high on every other high pulse of 2H (0.625 MHz).

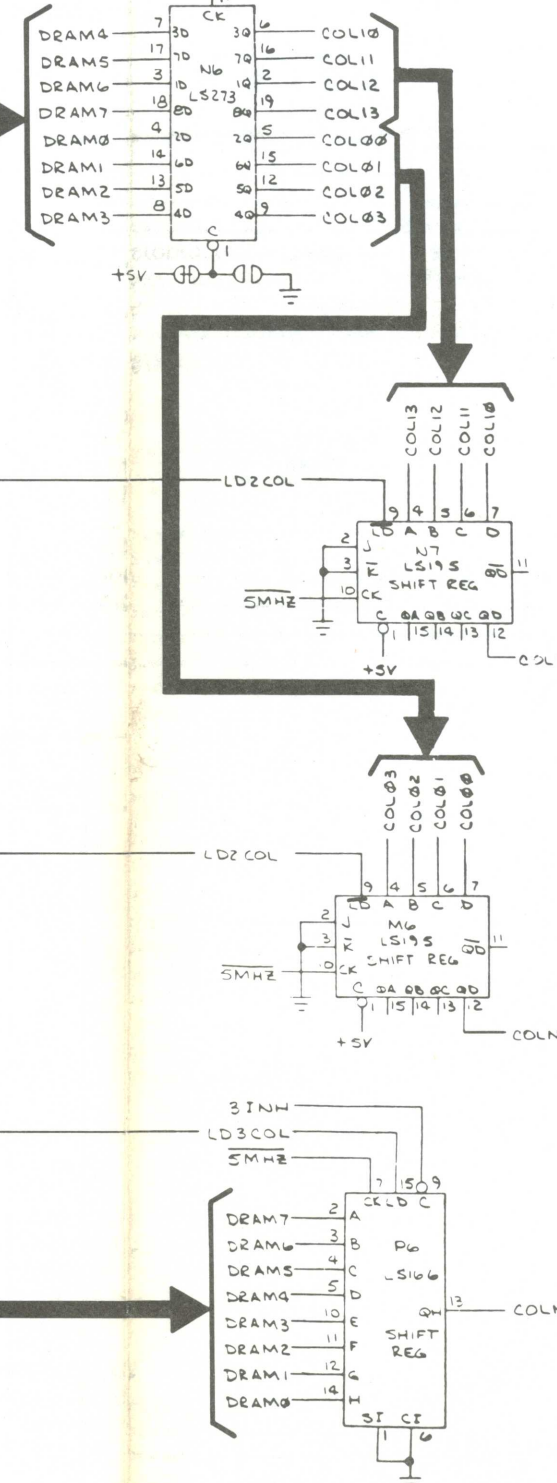
**$\Phi 0$  (Microprocessor Clock Input)** - Sync-generated signal, controlled by the microprocessor and sync that is the basic clock input to the microprocessor.

### DRAM Picture Output Enable



TO SHEET 1, SIDE B  
MICROPROCESSOR CIRCUIT

### Picture Bit Converter



**LD2COL (Load 2-Color picture bits)** - Sync-generated signal that, when low, loads 2-color parallel picture bits COLX into shifters M6 and N7 of the Picture Bit Converter Circuit. This signal occurs at twice the rate of LD3COL.

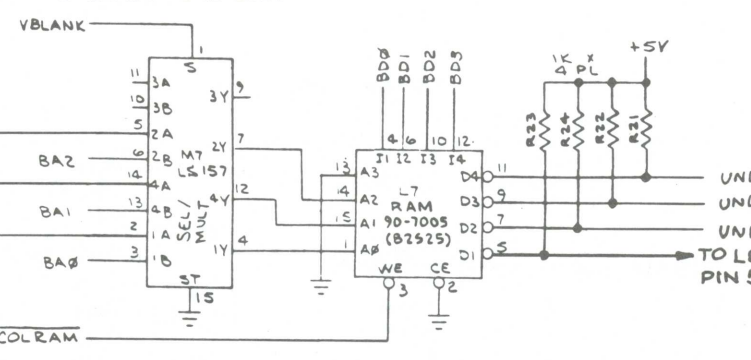
**LD3COL (Load 3rd Color picture bits)** - Sync-generated signal that, when low (3INH must be low) loads 3rd-color parallel picture bits DRAM0 thru DRAM7 into shifters P6 of the Picture Bit Converter Circuit. This signal occurs at one-half the rate of LD2COL.

**COLRAM (Color RAM write enable)** - Color RAM write enable generated by the Address Decoding Circuit. During the vertical blanking period (VBLANK period) COLRAM typically goes low. Microprocessor addresses color RAM L7 with BA0 thru BA2 and writes data into the color RAM on data lines BD0 thru BD3.

**COLLx (2-color bits)** - Parallel screen bit outputs, from the Picture Bit Converter Circuitry, to shift registers M6 and N7. Bits are latched at output of N6 and loaded into shift registers M6 and N7 when LD2COL goes low. When LD2COL goes high, serial color bits are clocked out at 5MHz rate.

**VBLANK (Vertical Blanking)** - Sync-generated signal that permits the microprocessor to access the Color RAM and write color commands during the vertical blanking period of the monitor display.

### Color RAM



**UNLBLUE (Unlatched Blue color signal)** - Unlatched blue color signal output of Color RAM.

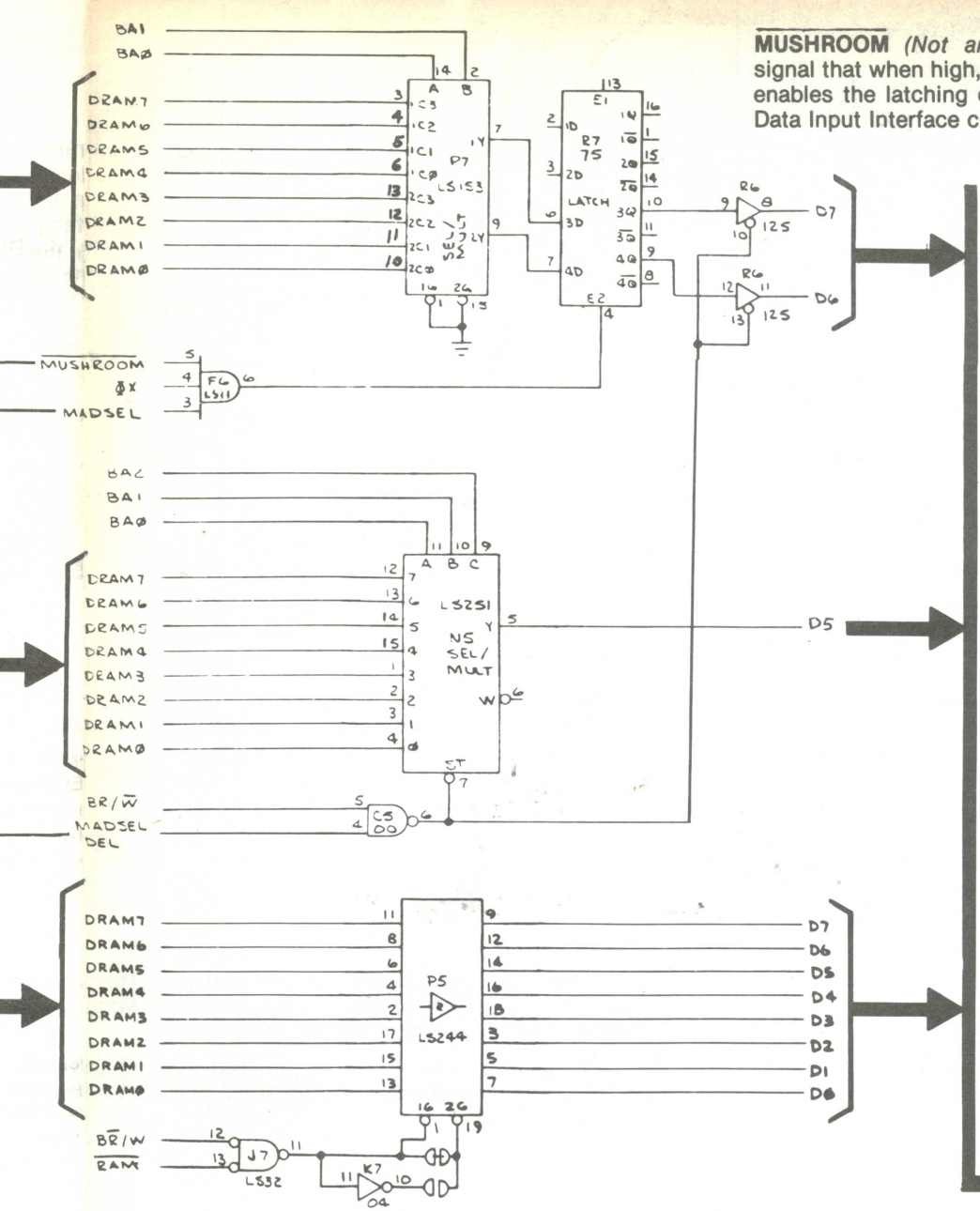
**UNLGREEN (Unlatched Green color signal)** - Unlatched green color signal output of Color RAM.

**UNLRED (Unlatched Red color signal)** - Unlatched red color signal output of Color RAM.

TO VIDEO OUTPUT CIRCUIT

TO SHEET 1, SIDE B  
ADDRESS DECODING CIRCUIT

### Microprocessor Data Input Interface



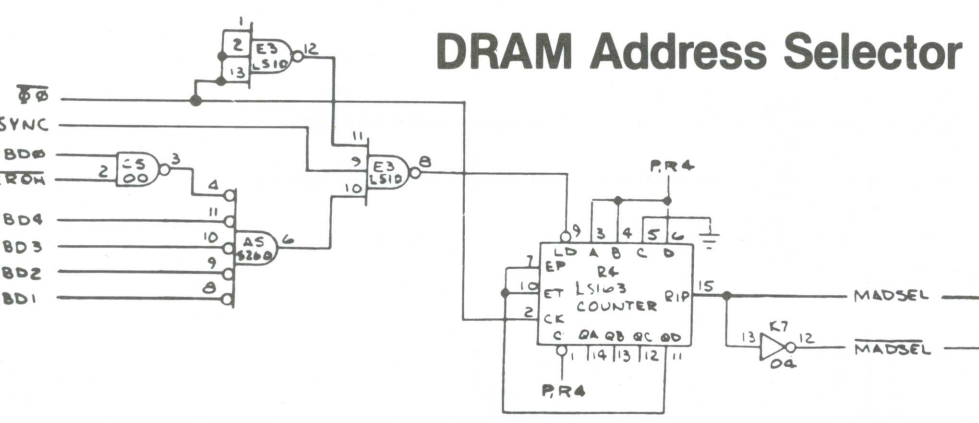
**3INH (Third-color bit inhibit)** - Sync-generated signal that, when high, prohibits a 3rd-color bit output from the Picture Bit Converter circuit. 3INH goes low during the last 32 scan lines (cities area) of the video display.

**MUSHROOM (Not an acronym)** - Microprocessor-generated signal that when high, along with high MADSEL and  $\Phi X$  signals, enables the latching of 2-color bit data in the Microprocessor Data Input Interface circuit.

TO MICROPROCESSOR UNSUPPLIED DATA LINE INPUT

**MADSELDEL (Multiplexed Address Select Delayed)** - Microprocessor-generated signal delayed one pulse of 5MHz from MADSEL signal. When MADSELDEL is high, along with high BR/W, microprocessor reads DRAM data output through Microprocessor Data Input Interface. MADSELDEL also disables Microprocessor Address Decoding Circuit.

**BR/W (Buffered Read/Write)** - Microprocessor-generated read/write signal used, along with RAM, to enable data port P5. When enabled, the microprocessor reads the working RAM area of the DRAM on data lines D0 thru D7.



### DRAM Address Selector

**MADSEL (Multiplexed Address Select)** - Microprocessor-generated signal that, when high, enables the microprocessor to write or read 2- or 3-color bit data into or out of the DRAM. MADSEL and MUSHROOM together select the address inputs, the data inputs and the actual DRAM chips to be written to or read from. MADSEL also, along with high MUSHROOM and  $\Phi X$  enables the latching of 2-color bit data in the Microprocessor Data Input Interface circuit. See tables in DRAM Write Enable and DRAM Data Input Selector circuits.

**SYNC** - Signal generated directly from the microprocessor that occurs at the beginning of an instruction read cycle and lasts one cycle of microprocessor  $\Phi 2$  clock. Five  $\Phi 0$  cycles later, MADSEL goes high.

MUSHROOM

MUSHROOM

MADSEL

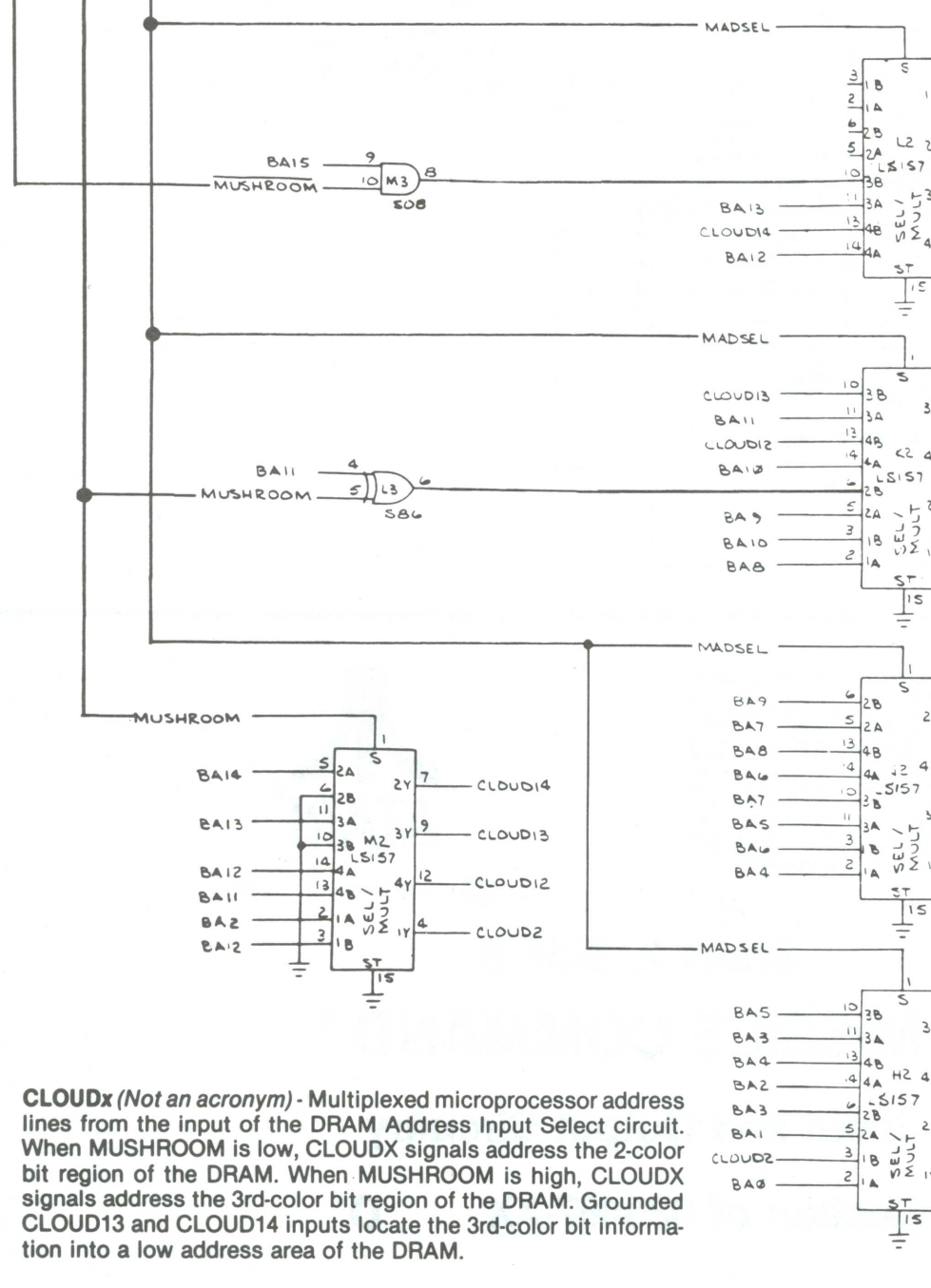
**BR/W (Buffered Read/Write)** - Microprocessor-generated signal that, when low (see RAM and MADSEL), enables the DRAM Write Enable Circuit to output high write pulses WPX to the DRAM. When high, along with a high MADSELDEL enables picture data to be read from Microprocessor Data Input Interface on data lines D5, D6 and D7.

**MUSHROOM (Not an acronym)** - Microprocessor-generated signal that, when high, enables the microprocessor to write or read the 3rd-color bit data into the DRAM. MUSHROOM and MADSEL together select the address inputs, the data inputs and the actual DRAM chips to be written to or be read from. See tables in DRAM Write Enable and DRAM Data Input Selector circuits.

**CAS (Column Address Strobe)** - Sync-generated strobe that, along with RAS and DEADSEL, sets up the address input to the DRAM. RAS sets up the seven row-address bits and latches the bit inputs for the DRAM row address. CAS sets up the seven column-address bits and latches the bit inputs for the DRAM column address. DEADSEL selects the origin of the seven address-bit inputs.

**DEADSEL (Address Select)** - Sync-generated strobe that, along with RAS and CAS, sets up the address input of the DRAM. RAS strobes the DRAM to latch the row-address inputs. CAS strobes the DRAM to latch the column-address inputs. When high, DEADSEL selects the row-address inputs. When low, DEADSEL selects the column-address inputs.

**RAS (Row Address Strobe)** - Sync-generated strobe that, along with CAS and DEADSEL, sets up the address input to the DRAM. RAS sets up the seven row address bits and latches the bit inputs for the DRAM row address. CAS sets up the seven column-address bits and latches the bit inputs for the DRAM column address. DEADSEL selects the origin of the seven address-bit inputs.



### DRAM Address Controller

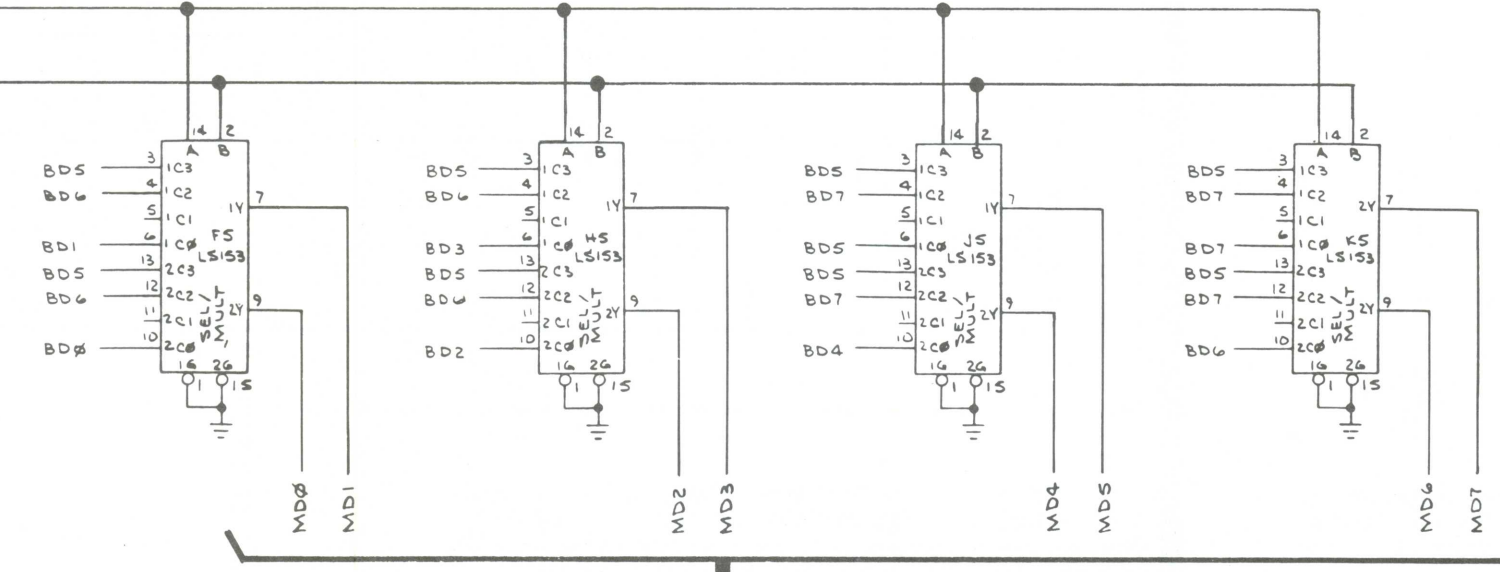
**MADx (Multiplexed Address)** - Address lines from microprocessor selected by MADSEL signal. When MADSEL is low, the MADx signals address the working RAM section of the DRAM with address lines BA0 thru BA13. When MADSEL is high, the MADx signals address the 2- or 3-color bit region of the DRAM.

**3COLSEL (Three Color Select)** - Sync-generated signal that switches the address of the DRAM from the 2-color bit region to the 3rd-color bit region of the DRAM during the last 32 scan lines (cities area) of the video display.

**CLOUDx (Not an acronym)** - Multiplexed microprocessor address lines from the input of the DRAM Address Input Select circuit. When MUSHROOM is low, CLOUDx signals address the 2-color bit region of the DRAM. When MUSHROOM is high, CLOUDx signals address the 3rd-color bit region of the DRAM. Grounded CLOUD13 and CLOUD14 inputs locate the 3rd-color bit information into a low address area of the DRAM.

**VAPORIZEX (not an acronym)** - Multiplexed sync lines at the input of the DRAM Address Input Selector circuit. When 3COLSEL is low, VAPORIZEX signals address the 2-color bit region of the DRAM. When 3COLSEL is high, VAPORIZEX signals address the 3rd-color bit region of the DRAM. Grounded VAPORIZEX11 and VAPORIZEX12 coincide with the grounded CLOUD13 and CLOUD14 microprocessor address inputs, permitting sync to access the 3rd-color bit information in the low address area of the DRAM.

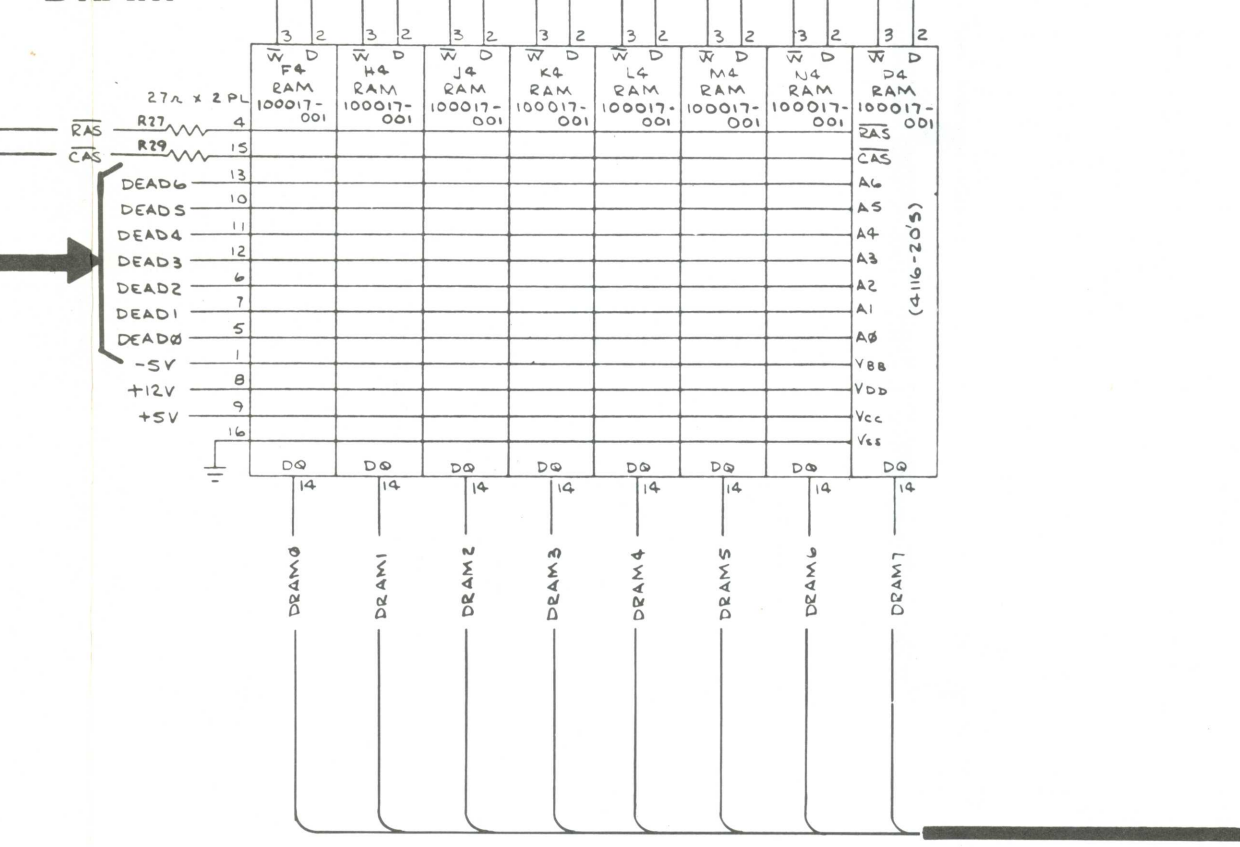
### DRAM Data Input Selector



**WPx (Write enable Pulses)** - Microprocessor-generated signals that select eight DRAM chips in the working RAM area of the DRAM, select one pair of DRAM chips in the 2-color bit region of the DRAM, or one DRAM chip in the 3rd-color bit region of the DRAM.

**MDx (Multiplexed Data)** - Data line to the DRAM from the microprocessor, selected by MADSEL and MUSHROOM signals. Table DRAM Data Input Selector Circuit defines source, controlled by MADSEL and MUSHROOM signals.

### DRAM



**DEADx (DRAM Address)** - Column- and row-address inputs to the DRAM selected by DEADSEL and  $\Phi X$ . When DEADSEL is high, DEADx signals are row-address inputs to DRAM. When DEADSEL is low, DEADx signals are column-address inputs to DRAM. When  $\Phi X$  is low, DEADx address inputs are from Sync Circuit. When  $\Phi X$  is high, DEADx address inputs are from microprocessor address lines.

**DRAMx (DRAM data output bits)** - Data output bits from the DRAM. The DRAMx signals are converted to serial data by the Picture Bit converter Circuit, then address the Color RAM. The microprocessor reads working RAM data DRAM0 thru DRAM7 through P5 in the Microprocessor Data Input Interface when RAM and BR/W are low. The microprocessor reads selected picture data bits when BR/W and MADSELDEL are high on data lines D5, D6 and D7.



Sheet 2, Side A  
**MISSILE COMMAND™**  
COCKTAIL  
Video Generator

Section of 035467-XX D

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