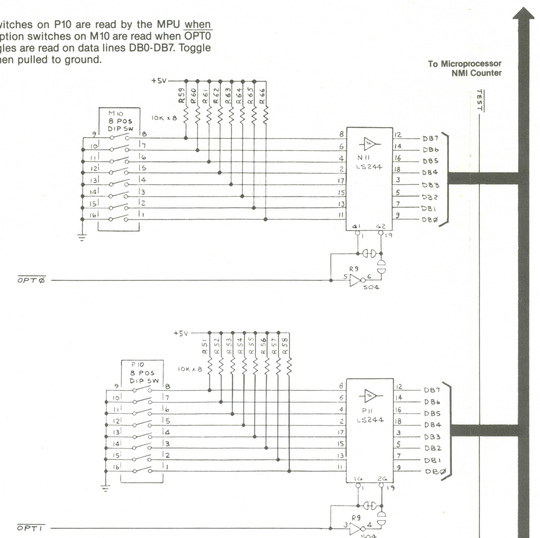
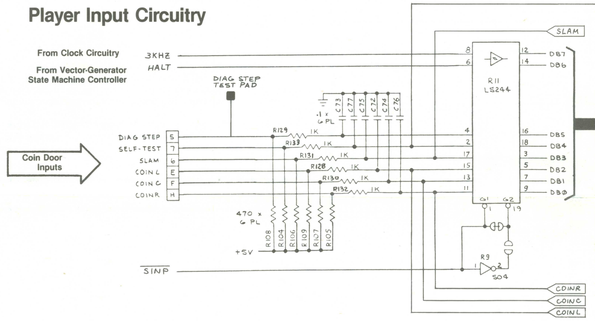
Option Switch Inputs

Game option switches on P10 are read by the MPU when OPT1 is low, and option switches on M10 are read when OPT0 is low. Switch toggles are read on data lines DB0-DB7. Toggle inputs are "on" when pulled to ground.



Player Input Circuitry



DIAG-STEP (diagnostic step), SELF-TEST, SLAM, COINL, COINC, COINR, 3KHz, and HALT inputs are read by the MPU when SINP (switch input) is low. The MPU reads these inputs on data lines DB0-DB7.

DIAG STEP, 3 KHz, and SELF-TEST are signals read by the MPU to initiate and control the game's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the antislam switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

ATARI®

Sheet 2, Side B

RED BARON™

Analog Vector-Generator Switch Input
Analog Vector-Generator Video Output
Analog Vector-Generator Coin Counter Output

Sheet 2, Side B
DP-171-02 1st printing

Analog Vector Generator PCB Output

The analog vector-generator output circuit consists of the X-axis, Y-axis and Z-axis video-output circuits, and a scaling circuit. The X- and Y-output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample-and-hold circuits and a video-output amplifier. The Z-axis output circuit consists of two input latches, a select multiplexer, and a summation network. The scaling circuit has an input latch, digital-to-analog converter and bias circuit.

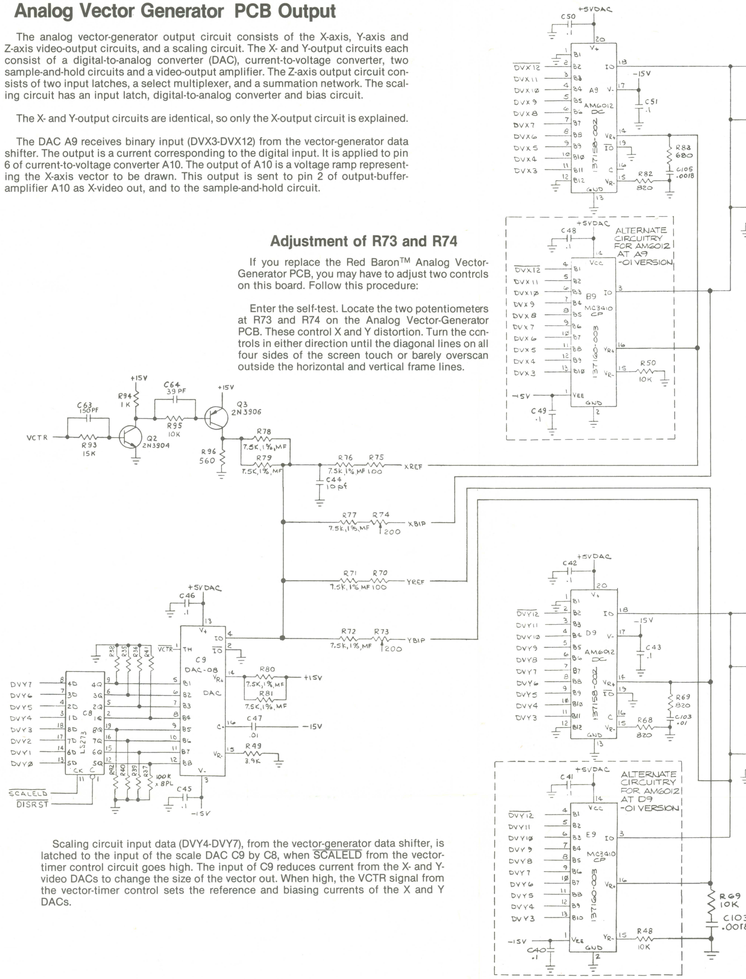
The X- and Y-output circuits are identical, so only the X-output circuit is explained.

The DAC A9 receives binary input (DVX3-DVX12) from the vector-generator data shifter. The output is a current corresponding to the digital input. It is applied to pin 6 of current-to-voltage converter A10. The output of A10 is a voltage ramp representing the X-axis vector to be drawn. This output is sent to pin 2 of output-buffer-amplifier A10 as X-video out, and to the sample-and-hold circuit.

Adjustment of R73 and R74

If you replace the Red Baron™ Analog Vector-Generator PCB, you may have to adjust two controls on this board. Follow this procedure:

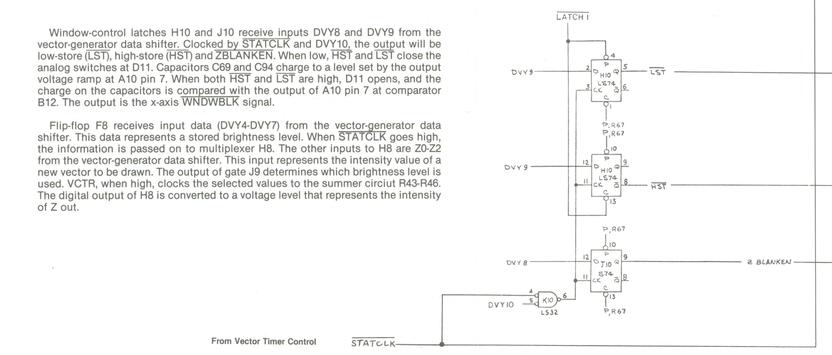
Enter the self-test. Locate the two potentiometers at R73 and R74 on the Analog Vector-Generator PCB. These control X and Y distortion. Turn the controls in either direction until the diagonal lines on all four sides of the screen touch or barely overscan outside the horizontal and vertical frame lines.



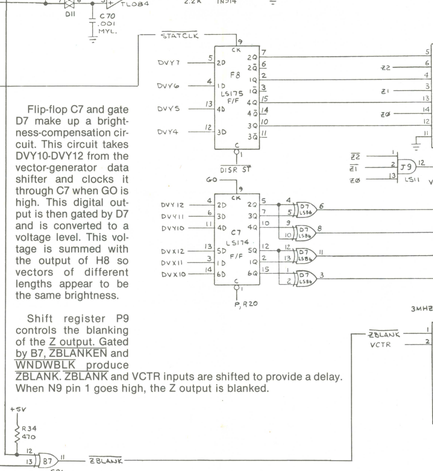
Scaling circuit input data (DVY4-DVY7), from the vector-generator data shifter, is latched to the input of the scale DAC C9 by C8, when SCALELD from the vector-timer control circuit goes high. The input of C9 reduces current from the X- and Y-video DACs to change the size of the vector out. When high, the VCTR signal from the vector-timer control sets the reference and biasing currents of the X and Y DACs.

Window-control latches H10 and J10 receive inputs DVY8 and DVY9 from the vector-generator data shifter. Clocked by STATCLK and DVY10, the output will be low-store (LST), high-store (HST) and ZBLANKEN. When low, HST and LST close the analog switches at D11. Capacitors C89 and C94 charge to a level set by the output voltage ramp at A10 pin 7. When both HST and LST are high, D11 opens, and the charge on the capacitors is compared with the output of A10 pin 7 at comparator B12. The output is the x-axis WNDWBLK signal.

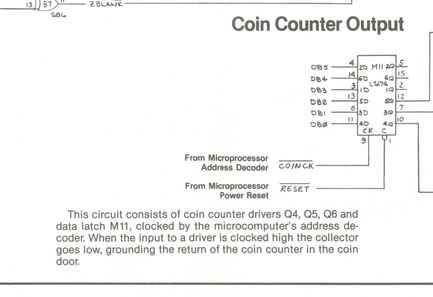
Flip-flop F8 receives input data (DVY4-DVY7) from the vector-generator data shifter. This data represents a stored brightness level. When STATCLK goes high, the information is passed on to multiplexer H8. The other inputs to H8 are Z0-Z2 from the vector-generator data shifter. This input represents the intensity value of a new vector to be drawn. The output of gate J9 determines which brightness level is used. VCTR, when high, clocks the selected values to the summer circuit R43-R46. The digital output of H8 is converted to a voltage level that represents the intensity of Z out.

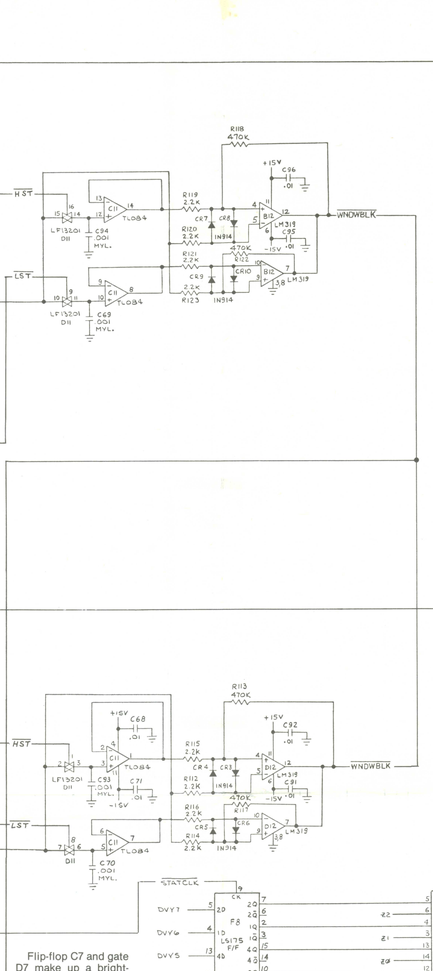


Flip-flop C7 and gate D7 make up a brightness-compensation circuit. This circuit takes DVY10-DVY12 from the vector-generator data shifter and clocks it through C7 when GO is high. This digital output is then gated by D7 and is converted to a voltage level. This voltage is summed with the output of H8 so vectors of different lengths appear to be the same brightness.

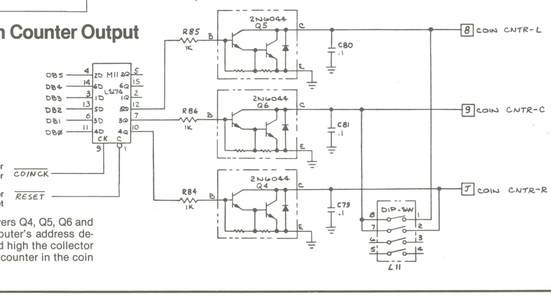


Shift register P9 controls the blanking of the Z output. Gated by B7, ZBLANKEN and WNDWBLK produce ZBLANK. ZBLANK and VCTR inputs are shifted to provide a delay. When N9 pin 1 goes high, the Z output is blanked.





Coin Counter Output



This circuit consists of coin counter drivers Q4, Q5, Q6 and data latch M11, clocked by the microcomputer's address decoder. When the input to a driver is clocked high the collector goes low, grounding the return of the coin counter in the coin door.