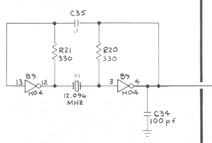
## CLOCK



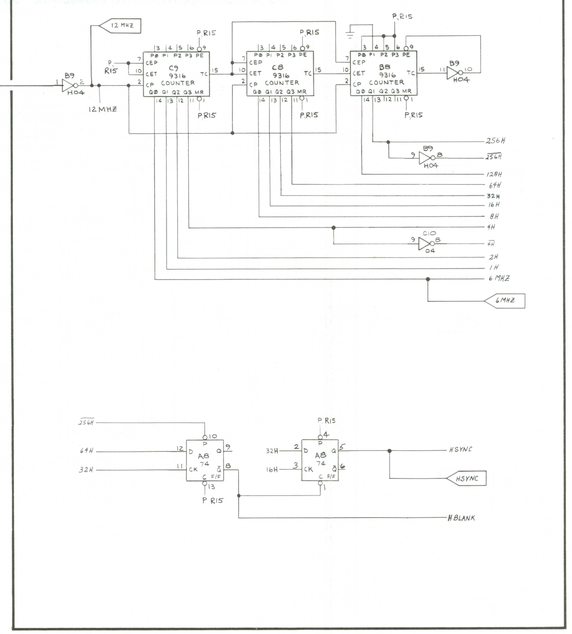

The basic frequency of the sync generator is a 12.096 MHz clock, generated by crystal Y1. The output of the oscillator, viewed with an oscilloscope, is a signal with a period of 83 nanoseconds.

The oscillator frequency is divided down by binary counters C9, C8, and B8. These provide various horizontal synchronization frequencies (1H thru 256H). The final output of the horizontal counting chain is 256H. This signal is, in effect, a division of the oscillator frequency by 768, or 15,750 Hz. The period of 256H is about 63.5 microseconds. The 256H signal, as well as other horizontal signals, are used to generate H BLANK and H SYNC timing pulses.

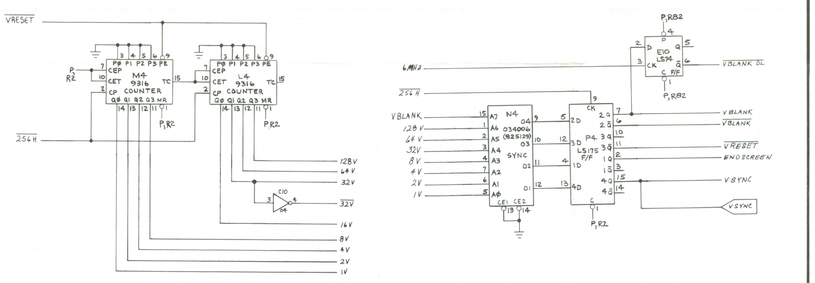
The 256H signal is used to generate vertical sync signals 1V thru 128V. The 128V signal is, in effect, a division of the 256H frequency by 262. This results in the final output from the counters of 60 Hz (16.6 milliseconds). The various vertical sync signals address sync PROM N4 whose data is latched at the output of P4.

The end result of the horizontal and vertical timing waveform is to synchronize the TV monitor display. This display consists of 262 horizontal lines per frame; only 240 lines are visible, since the last 22 lines occur during vertical blanking. Each line is equivalent to 768 clock pulses. Each frame is repeated 60 times per second, providing the necessary frequency of display refresh for a stable, non-flickering display.

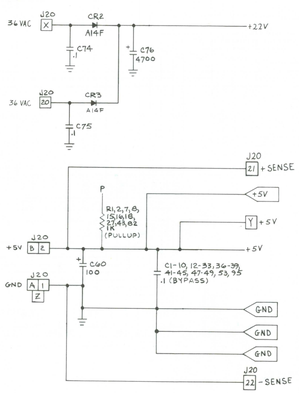
## HORIZONTAL SYNC




## VERTICAL SYNC

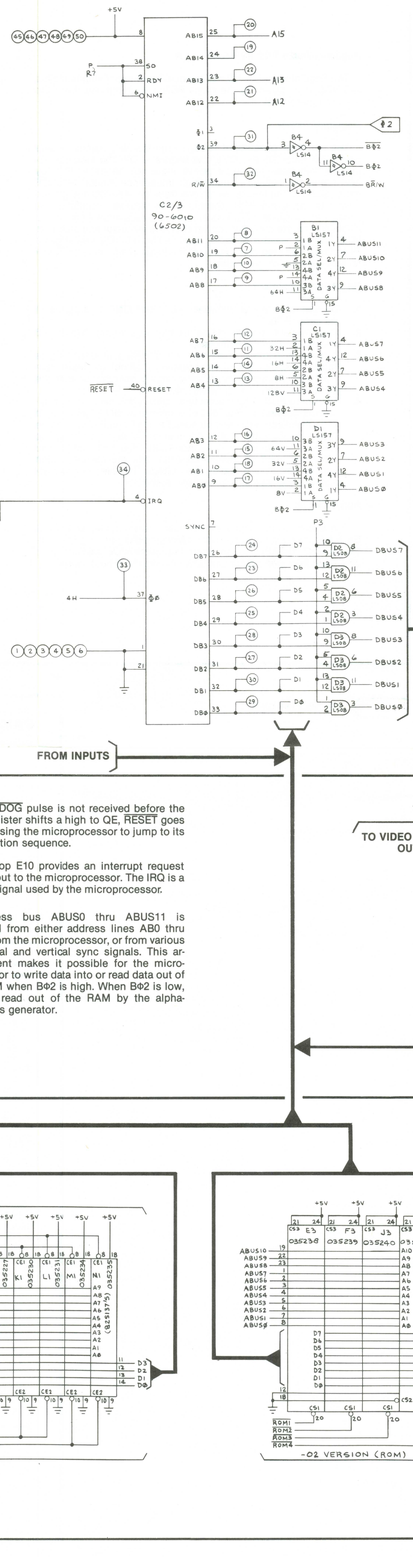



## POWER INPUT

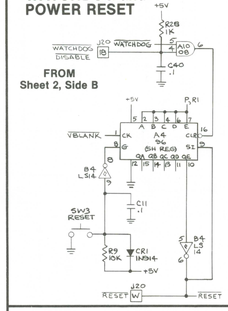



Sheet 1, Side B
DP-144-01 1st printing

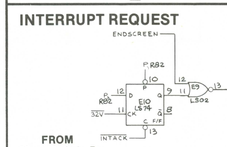
## MICROPROCESSOR




### WATCHDOG and POWER RESET




### INTERRUPT REQUEST




The microprocessor controls all circuits on the game PCB, excluding the Sync Circuit and Watchdog and Power Reset Circuit. The Sync Circuit provides 4H (750 KHz) for the Φ0 clock input to the microprocessor.

The Watchdog and Power Reset Circuit forces the microprocessor into its initialization sequence during initial power-up, or if the program strays from its normal sequence. When power is initially applied to the PCB, capacitor C11 and resistor R9 form a time constant that forces RESET low until the +5 VDC logic power becomes stable.

During normal operation, the microprocessor outputs address 1005 (hexadecimal) that is decoded by the address decoder for the WATCHDOG signal. This signal is received at the pin 5 input of A10. The signal input causes pin 16 of shift register A4 to go low which resets the shift register to a zero output. If the WATCHDOG pulse is not received before the shift register shifts a high to QE, RESET goes low, causing the microprocessor to jump to its initialization sequence.

Flip-flop E10 provides an interrupt request (IRQ) input to the microprocessor. The IRQ is a timing signal used by the microprocessor.

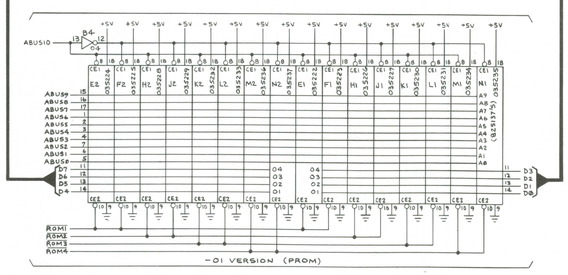
Address bus ABUS0 thru ABUS11 is selected from either address lines AB0 thru AB11 from the microprocessor, or from various horizontal and vertical sync signals. This arrangement makes it possible for the microprocessor to write data into or read data out of the RAM when Bϕ2 is high. When Bϕ2 is low, data is read out of the RAM by the alphanumerics generator.

denotes a test point

## ROM/PROM MEMORY

Your Atari Soccer game PCB may contain one of several possible program memory chips sets. The -01 version of the PCB contains 16 PROMs for the memory.

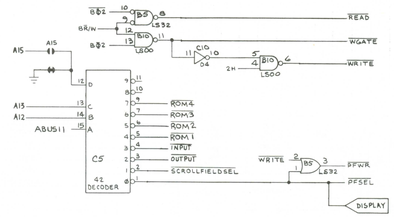
The -02 version contains 4 ROM chips for the memory. A third possibility would be a mixture of ROMs and PROMs. For information regarding which ROMs are equivalent to which PROMs, see the Illustrated Parts Catalog chapter of the game manual.







## ADDRESS DECODER




The address decoder receives addresses from the microprocessor, decodes the addresses, and turns on the required circuitry for carrying out the instruction for that address. The address map below is for the Atari Soccer game. This map provides the necessary information for operating the circuitry with the Atari Automatic ROM/RAM Tester. Before connecting the Tester, do the following:

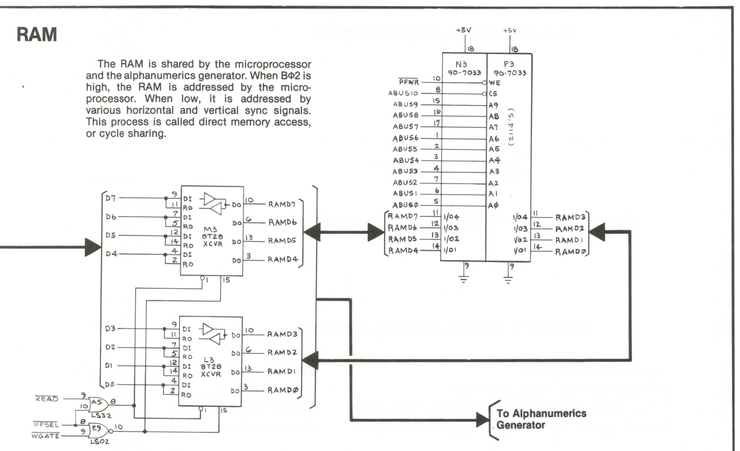
1. Remove the microprocessor.
2. Short pin 37 to 39 of microprocessor socket C2/3.
3. Ground pin 18 of edge-connector J20.

The ones and zeros in the ADDRESS column of the address map indicate the address necessary for information to be passed to and from the microprocessor. A 0 indicates that the address line is low, and a 1 indicates the line is high. Blank spaces indicate that it doesn't matter whether the address line is low or high. An A indicates that the address line is used as part of the functional address for that particular peripheral access. In the DATA column, a D indicates that the data line is used to transfer information.

| HEXADECIMAL | ADDRESS A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | DATA D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0000-01FF | | | 0 | 0 | 0 | 0 | 0 | A | A | A | A | A | A | A | A | A | | D | D | D | D | D | D | D | D | WORKING RAM |
| 0200-03FF | | | 0 | 0 | 0 | 0 | 1 | A | A | A | A | A | A | A | A | A | | D | D | D | D | D | D | D | D | ALPHA NUMERICS |
| 0800-08BF | | | 0 | 0 | 1 | 0 | A | A | A | A | A | A | A | A | A | A | | D | D | D | D | D | D | D | D | PLAYFIELD OBJECTS |
| 08C0-08FF | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | A | A | A | A | | D | D | D | D | D | D | D | D | MOTION OBJECTS |
| 0BC0-0BDE | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | A | A | A | A | 0 | D | D | D | D | D | D | D | D | MOTION OBJECT PICTURE NUMBER |
| 0BC1-0BDF | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | A | A | A | A | 1 | | D | D | D | D | D | D | D | MOTION OBJECT VERTICAL POSITION |
| 0BE0-0BFE | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | A | A | A | A | 0 | D | D | D | D | D | D | D | D | MOTION OBJECT HORIZONTAL POSITION |
| 0BE1-0BFF | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | A | A | A | A | 1 | | | D | D | | | | | D5, D4 AREA 3 GRAY |
| 0BE1-0BFF | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | A | A | A | A | 1 | | | | | D | D | | | D3, D2 AREA 2 GRAY |
| 0BE1-0BFF | | | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | A | A | A | A | 1 | | | | | D | D | | | D1, D0 AREA 1 GRAY |
| 1000 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | D | D | D | D | D | D | D | SCROLLFIELD OFFSET LATCH (OUT1) |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 1 | W | D | | | | | | | RULE LED |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | | | D | | | | | CONTROL SIGNAL FOR TRACKBALL LD2 |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | | | | D | | | | CONTROL SIGNAL FOR TRACKBALL LD1 |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | | | | | D | | | 4/2 PLAYER LED |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | | | | | | D | | SPARE |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | | | | | | | D | KICKER NOISE GENERATOR INITIALIZE |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | | | | | | D | | HIT SOUND |
| 1001 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | | | | | | | D | WHISTLE SOUND |
| 1002 | | | 0 | 1 | 0 | | | | | | | | | | | | 0 | W | D | | | | | | | AMP OFF |
| 1002 | | | 0 | 1 | 0 | | | | | | | | | | | | 1 | W | | D | D | D | | | | COIN COUNTER LEFT, CENTER, RIGHT |
| 1004 | | | 0 | 1 | 0 | | | | | | | | | | | | 1 | W | | | | D | D | D | D | AUDIO OUTPUT CONTROL |
| 1005 | | | 0 | 1 | 0 | | | | | | | | | | | | 1 | W | | | | | | | | INTERRUPT ACKNOWLEDGE |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | D | | | | | | | WATCHDOG REFRESH |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | D | | | | | | D7 RT PLY 2 VERT DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | D | | | | | D6 RT PLY 2 HORZ DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | D | | | | D5 LT PLY 2 VERT DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | | D | | | D4 LT PLY 2 HORZ DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | | | D | | D3 RT PLY 1 VERT DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | | | | D | D2 RT PLY 1 HORZ DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | | | | | D1 LT PLY 1 VERT DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | | | | | D0 LT PLY 1 HORZ DIR LD2 = 0, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | D | D | D | D | | | | D7-D4 RT PLY 1 VERT TRACKBALL LD2 = 1, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | | D | D | D | D3-D0 RT PLY 1 HORZ TRACKBALL LD2 = 1, LD1 = 0 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | D | D | D | D | | | | D7-D4 RT PLY 2 VERT TRACKBALL LD2 = 1, LD1 = 1 |
| 1800 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | R | | | | | D | D | D | D3-D0 RT PLY 2 HORZ TRACKBALL LD2 = 1, LD1 = 1 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | D | | | | | | D7 SWITCH 0 LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | D | | | | | D6 SWITCH 1 LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | D | | | | D5 SWITCH 2 LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | | D | | | D4 SWITCH 3 LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | | | D | | D3 OPTION SW LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | | | | D | D2 OPTION SW LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | | | | | D1 RULE SWITCH LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | | | | | D0 4/2 PLAYER SWITCH LD2 = 0, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | D | D | D | D | | | D7-D4 LT PLY 1 VERT TRACKBALL LD2 = 1, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | | | D | D | D3-D0 LT PLY 1 HORZ TRACKBALL LD2 = 1, LD1 = 0 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | D | D | D | D | | | D7-D4 LT PLY 2 VERT TRACKBALL LD2 = 1, LD1 = 1 |
| 1802 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 0 | R | | | | | D | D | D3-D0 LT PLY 2 HORZ TRACKBALL LD2 = 1, LD1 = 1 |
| 1801 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | 1 | R | D | | | | | | ENDSCREEN |
| 1801 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | 1 | R | | D | | | | | TEST |
| 1801 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | 1 | R | | | D | | | | SLAM |
| 1801 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | 1 | R | | | | D | | | COIN LEFT |
| 1801 | | | 0 | 1 | 1 | | | | | | | | | | | | 0 | 1 | R | | | | | D | | COIN CENTER |
| 1801 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 1 | R | | | | | | D | COIN RIGHT |
| 1803 | | | 0 | 1 | 1 | | | | | | | | | | | | 1 | 1 | R | D | D | D | D | D | D | OPTION SWITCH |
| 2000-3FFF | | | 1 | A | A | A | A | A | A | A | A | A | A | A | A | A | R | D | D | D | D | D | D | D | D | PROGRAM SPACE |

## RAM

The RAM is shared by the microprocessor and the alphanumerics generator. When Bϕ2 is high, the RAM is addressed by the microprocessor. When low, it is addressed by various horizontal and vertical sync signals. This process is called direct memory access, or cycle sharing.






ATARI
A Warner Communications Company

**Sheet 1, Side B**

**SOCCER**

**Microcomputer, Clock, and Sync**

**034905-XX A**