VIDEO GENERATOR

FROM MPU DATA BUS

The address decoder outputs the scrollfield write enable signal $\overline{SFWR}$, and the microprocessor selects the appropriate RAM pair with address lines ABUS0 and ABUS5.

VIDEO GENERATOR RAM

When the RAM is written to by the microprocessor, $\overline{SFWR}$ is low and a RAM pair is written to by the selection of ABUS0 and ABUS5. Data is written into the RAM through data bus DBUS0 thru DBUS7. Data is read out of the RAM on data lines PFD0 thru PFD31.

Data Selectors F4, H4, J4 and K4 select the addressing mode for the Video Generator RAM. When 4H is high, the MPU addresses the RAM, via ABUS 0-9. When 4H is low, the Video Generator RAM is addressed by either the scrollfield horizontal address (SFH 3-7) or by the sync chain (8H-64H and 16V-128V). 256H determines which of these two addresses the RAM when 4H is low. When 256H is low, sync is selected for motion objects scan. When 256H is high, scrollfield is selected.

The latched data output of D4 is compared with horizontal sync 8H thru 64H, to enable the playfield to scroll (shift) in steps of 8H. SFH0 thru SFH2 selects the scrollfield output from multiplexer D8 in steps of 1H.

From Sheet 1, Side B

When 256* is high, playfield object graphics data is read out of Graphics ROM R6 (PROMs R7 and R8 for -01 version). During this period, the $\overline{256H*}$ signal enables data selectors R9, P9, M8 and N8.

PIC0 thru PIC5 select 64 different pictures. GA6 thru GA9 select the actual line of the picture to be output. When PIC7 goes high, GA6 thru GA9 are inverted, resulting in the monitor display being inverted vertically. When PIC6 goes high, MASKA and MASKB signals are inverted, resulting in the monitor display being inverted horizontally.

GRAPHICS PROM R6 also contains playfield object graphics data which is scanned during 256H* high.

Signals SFH0 thru SFH2 select the scrollfield output (MASKA) in steps of 1H.

When 256H* is low, motion object graphics data is read out of Graphics ROMs, R6 and N6 (PROMs R7, R8, P7, P8, N7 and M7 for -01 version) when MATCH is low. MASKA and MASKB define different areas of the motion object picture. The actual shading of the picture is assigned later with PFD25 thru PFD28 by multiplexers E8 and L9.

Adders L5 and M5 compare the vertical line presently being scanned with RAM data PFD8 thru PFD15, which defines the vertical location of the motion object. When the inputs are equal, MATCH is latched low, permitting the motion object data to be output from the graphics PROM. GA6 thru GA9 count up for the 16 scan lines of the motion object picture during 256H* low, otherwise it passes vertical count 1V thru 8V during 256H* high for playfield scan.

Motion object video data is written into RAM F9 and H9 when 256H* is low. Signals PFD16 thru PFD23, latched at the output of flip-flop J8, define the starting location of the motion object(s) along the horizontal line. The HAD0 thru HAD7 signals address high-speed RAMs F9 and H9 for each of the sixteen counts of counters J9 and K9 for each motion object. The data written into the RAMs is color coded by the selection of signals PFD24 thru PFD29 selected by MASKA and MASKB through multiplexer E8.

At the beginning of the actual scan line, the counters are cleared and start counting from 0 to 255. Data written into RAMs F9 and H9 are read out of locations addressed by HAD0 thru HAD7.

GRAY0LATCH and GRAY1LATCH select the playfield or the shading of motion objects by selecting the inputs of multiplexer L9. When both GRAY0LATCH and GRAY1LATCH are low, playfield objects are output. When GRAY0LATCH is high and GRAY1LATCH is low, black motion objects are output. When GRAY0LATCH is low and GRAY1LATCH is high, gray motion objects are output. When GRAY0LATCH and GRAY1LATCH are both high, white motion objects are output.

ALPHANUMERICS GENERATOR

From Sheet 1, Side B

The alphanumerics at both ends of the monitor display are generated by alphanumerics PROM R2. This PROM is addressed by latched MPU RAM data signals RAMD0 thru RAMD7. The MPU writes alphanumerics data into the MPU RAM during the Φ2 periods. During the Φ2 periods the MPU RAM is accessed by horizontal and vertical sync signals. The latched MPU RAM data RAMD0 thru RAMD5, selects one of the 64 possible characters. The latched RAMD7, low data, enables the alphanumerics PROM R2. RAMD6 is used to invert the data output of the PROM both horizontally and vertically. The signal at the input of shift register P1 ensures that the generated alphanumerics only appear at each end of the monitor display.

The alphanumerics, playfield, motion objects video and vertical and horizontal sync signals are all summed at the video summer. The VBLANKDL signal ensures that there is no video during the vertical blanking period.

denotes a test point

Sheet 2, Side A
SOCCER
Video Generator and Alphanumerics Generator

ATARI®

A Warner Communications Company

Sheet 2, Side A
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