

# Bally Midway's MCR I I I

Notes from DLH on Jan 19<sup>th</sup>, 2000

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Schematics scanned at 600 dpi/lineart  
All other at 300 dpi/lineart

This manual had the same exact first 19 pages as the manual  
for MCR I I (MCR2-Part1.pdf & MCR2-Part2.pdf)

Page 20 was blank

Page 31 doesn't exist in my original copy  
\*if someone has it, please scan or email me

You can not imagine what a pain these yellow  
Schematics were to scan ☹️

Enjoy

**Bally Midway's**  
**MCR II-III Systems**

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**General Information and  
Troubleshooting Procedures  
Micro-Processor Video Games**

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**Bally MIDWAY MFG. CO.**

10601 W. Belmont Avenue  
Franklin Park, Illinois 60131  
U.S.A.



Phone: (312) 451-9200 Cable Address: MIDCO Telex No.: 72-1596  
VIDEO 800/323-7182 PINBALL 800/323-3555

July, 1983

Form No. 00381-8306

## GAME VOLUME ADJUSTMENT CONTROL. (See Figure 1 )

The game volume control pot is located just inside the cabinet on the right side of the coin door frame. There is only one pot. For adjustment, it may be reached through the coin door on **ALL** models.

To make the sounds louder, turn the pot clockwise as you face it ( ↻ ).

To make the sounds **less** loud, turn the pot counter-clockwise as you face it ( ↺ ).

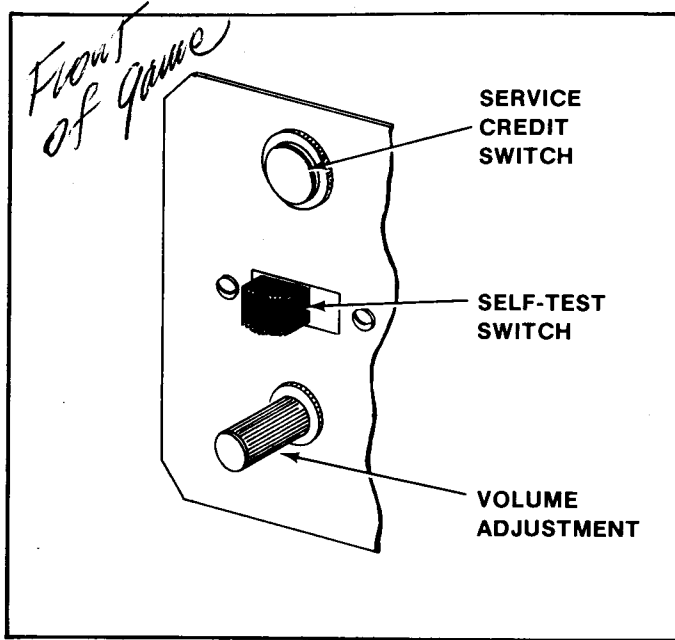


Figure 1 Game Volume Adjustment Control

## OPTION SETTINGS:

To change the most common option settings, you **DO NOT** have to take the game apart or go into the cabinet and hunt for tiny switches on P.C. boards. These most common options can be changed from the main console of the game while it is in the Self-Test mode. The Self-Test switch is located just inside the cabinet on the right side of the coin door frame as you face it.

When changing any options, **ALWAYS** perform the Self-Test and play the game to be sure the ones selected are working properly. Of course, when you must change one of the switches that is located on one of the game's P.C. boards, it is also recommended that you perform the Self-Test and play the game to be sure the switches have worked properly and that no switches were accidentally moved that were not meant to be. (These switches are small and this can happen.)

The P.C. Board option switch settings, and what they will make the game do are shown in Figure 3. These switches are **MAINLY INTENDED** for use by a technician who is checking and/or performing tests on the game. See Figure 2 for option switch locations.

**NOTE:** In order to set the option switches located on the game's P.C. Boards, these Boards need not be removed from their card rack.

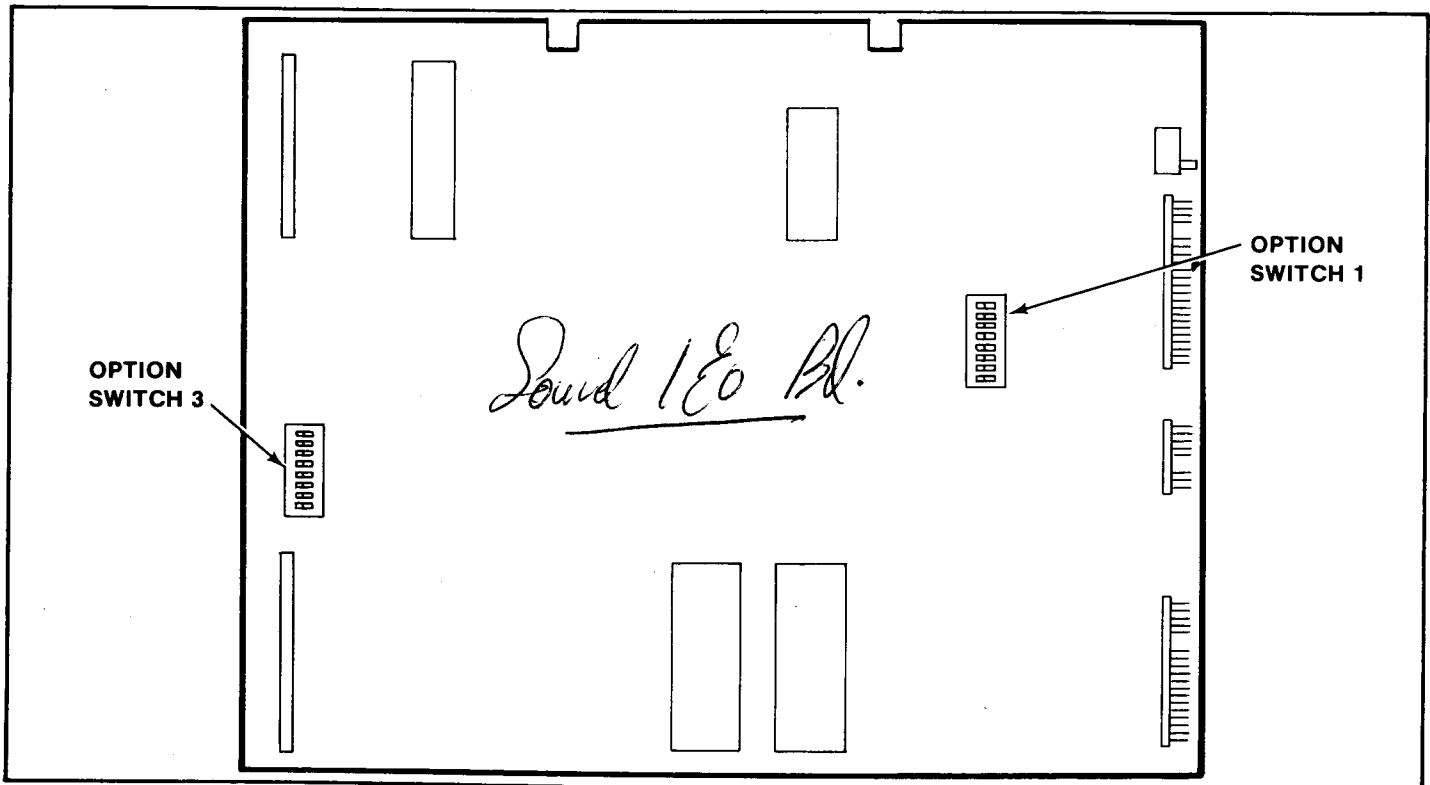


Figure 2 Option Switch Location

## OPTION SWITCH SETTINGS

### SWITCH NO. 1 — AT B 3 — LOCATED ON SOUND I/O P.C. BOARD

	SW#1	SW#2	SW#3	SW#4	SW#5	SW#6	SW#7	SW#8	SW#9	SW#10
2 COIN METERS 1 COIN METER	ON			NOT	NOT	NOT	NOT	NOT	NOT	NOT
	OFF			USED	USED	USED	USED	USED	USED	USED
MINI/UPRIGHT COCKTAIL TABLE	<b>ON</b> <b>OFF</b>	<i>Change picture Flip up</i>								
BUY IN ALLOWED NO BUY IN ( <i>Explain</i> )										
FREEZE VIDEO NORMAL OPERATION										<b>ON</b> <b>OFF</b>
										<i>Bench Aid - must be off</i>

### SWITCH NO. 3 — AT D 14 — LOCATED ON SOUND I/O P.C. BOARD *(Bench testing)*

	SW#1	**SW#2	**SW#3	**SW#4
NORMAL OPERATION SOUND I/O DIAGNOSTIC MODE	OFF			
	ON			
NORMAL OPERATION RAM/ROM TEST INDICATES TEST RESULTS VIA YELLOW LED ON SOUND I/O BOARD: <b>FAST FLASH = BAD ROM</b> <b>SLOW FLASH = BAD RAM</b>		OFF	THE REMAINDER OF MOST COMMON OPTION SETTINGS ARE CON- DUCTED DURING THE <b>MACHINE SETUP</b> PORTION OF THE SELF-TEST MODE AND WILL BE COVERED IN DETAIL IN THAT SECTION OF THIS MANUAL	
		ON		
NORMAL OPERATION OSCILLATOR TEST			OFF	
			ON	
NORMAL OPERATION FILTER TEST				OFF
				ON

\*\*NO EFFECT IF SW#1 OF SWITCH NO. 3 IS IN THE "OFF" POSITION.

Figure 3 Option Switch Settings

## SELF-TEST MODE

The Self-Test mode is a special mode for checking game play statistics as well as game switches and computer functions. It is the easiest and best way to check for proper operation of the entire game.

**NOTE:** Putting the game into Self-Test **WILL NOT** cause the game to erase any CREDITS it has in its memory when the Self-Test mode is entered.

You may begin a Self-Test at any time by sliding the Self-Test switch to the "ON" position after the power to the game is on (the Self-Test switch is located just inside the cabinet on the right side of the coin door frame as you face it). When this is done, the game will react as follows:

1. If the game is in the Attract mode when the Self-Test switch is moved to the "ON" position, it will finish the sequence and then go into the Self-Test mode. This is illustrated by the display of the Self-Test Mode Menu on the monitor screen.
2. If the game is in the Ready-To-Play mode or the Play mode when the Self-Test switch is slid to the "ON" position, it **WILL NOT** go into the Self-Test mode until **AFTER** the players' last TRON has been eliminated (the game **MUST** be over). At this point, the game will go into the Self-Test mode. Again, this is illustrated by the display of the Self-Test Mode Menu on the monitor screen.
3. The fastest way to enter the Self-Test mode is to slide the Self-Test switch to the "ON" position and then activate the "TILT" switch located on the back side of the coin door just below the lock mechanism. The game will then **IMMEDIATELY** go into the Self-Test mode.

The Self-Test mode has eight (8) major categories as illustrated by Figure 4.

1. It is easy to select what category you want to enter. By pushing forward or pulling backward on the controller stick, the Cursor at the left of the screen can be moved UP and DOWN, (forward=UP) and (backward=DOWN), until it is in front of the category you want to test. Release the controller stick at this time.
2. After the Cursor has been positioned, pull the trigger on the controller stick and the monitor screen will display the test category you have selected.

**NOTE:** There is one exception to this. If you position the Cursor in front of the "PRESET" category on the Self-Test Mode Menu, when you pull the trigger on the controller stick — **EVERYTHING**, I repeat — **EVERYTHING**; including **ALL** information in the "BOOKKEEPING" mode, and **ALL operator selected options**, will be set back to zero "0" and to the factory recommended settings — **respectively**.

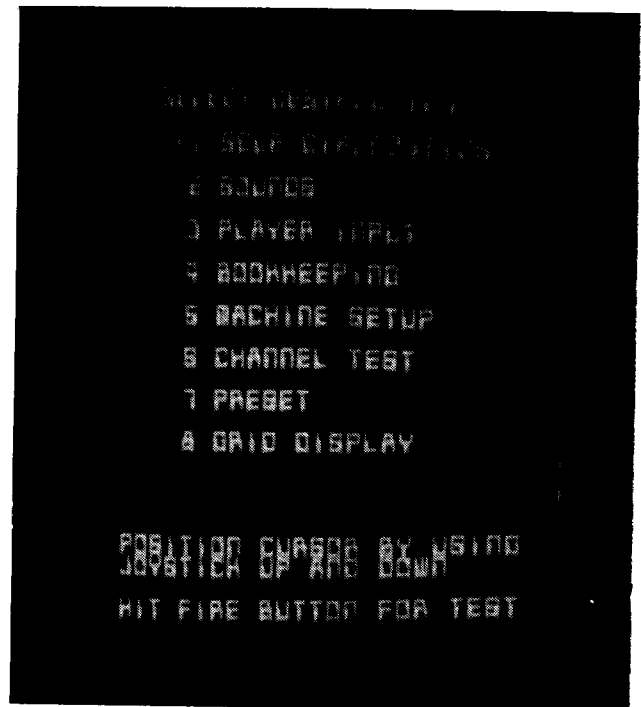


Figure 4 Self-Test—Menu

- Once you are **IN** one of the Self-Test mode categories, FOLLOW THE **ON-SCREEN INSTRUCTIONS** TO **COMPLETE** THE TEST.

3. The next group of figures shows the **CORRECT** screen presentation for **EACH** category of the Self-Test mode.

During the SELF DIAGNOSTICS section of the Self-Test mode, you will **first** see a cross hatch pattern on the screen for about 1/2 second. **Second**, you will see a lot of different colored bars shown on the monitor screen. These bars will be UNpainted one at a time from the top down. **Third**, you will see the screen painted Red, Blue, and Green in bars from the top down. **Fourth**, another group of colored bars is displayed. This sequence is repeated several times. And finally, this sequence is replaced by this message: "**HIT FIRE BUTTON TO EXIT**". If the Fire button is not hit, the test will repeat itself. This feature was designed into the game to enable over-night testing for an intermittent hardware problem.

If the SELF DIAGNOSTICS find one or more bad ROM or RAM chips: instead of going through what is described above, the game will give you a written message as to which parts are bad. This message includes their I.D.'s and their P.C. Board locations.

During the SOUNDS sections of the Self-Test mode, the game will give a display which looks like that shown in Figure 5.

- In this category, each of the game's 24 separate sounds can be checked individually in any order — or — you can tell the game to check them all in order — 3 through 26.

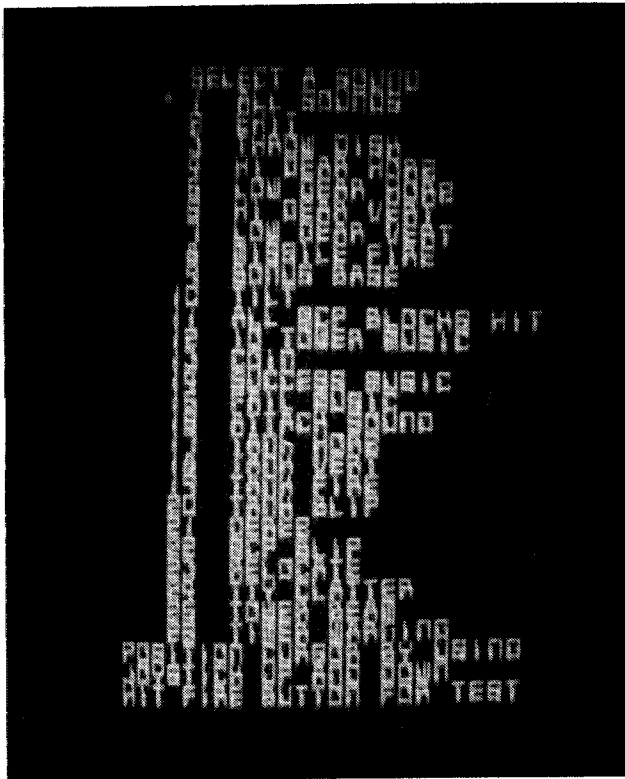


Figure 5 Self-Test—Sounds

As the Player Input Switches and Devices are activated, the Switch or Device activated is spelled out in the space indicated.

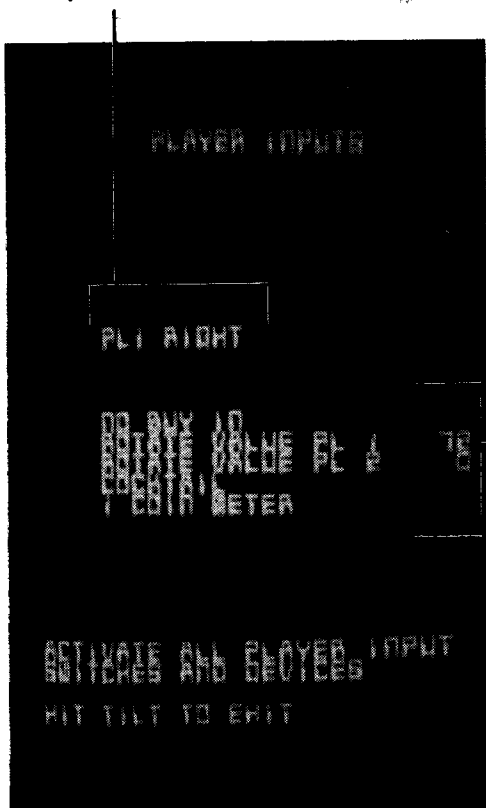


Figure 6 Self-Test—Player Input

This is a P.C.B. switch setting.

During the PLAYER INPUT section of the Self-Test mode, the game will give a display which looks like that shown in Figure 6.

- In this category, each of the game's player operated controls — including the coin switches on the back side of the coin door — may be checked individually. A game sound will be heard as each switch/control is actuated. If no game sound is heard, that switch/control is either not working, miswired, or disconnected. Check it out thoroughly.

During the BOOKKEEPING section of the Self-Test mode, the game will give a display which looks like that shown in Figure 7.

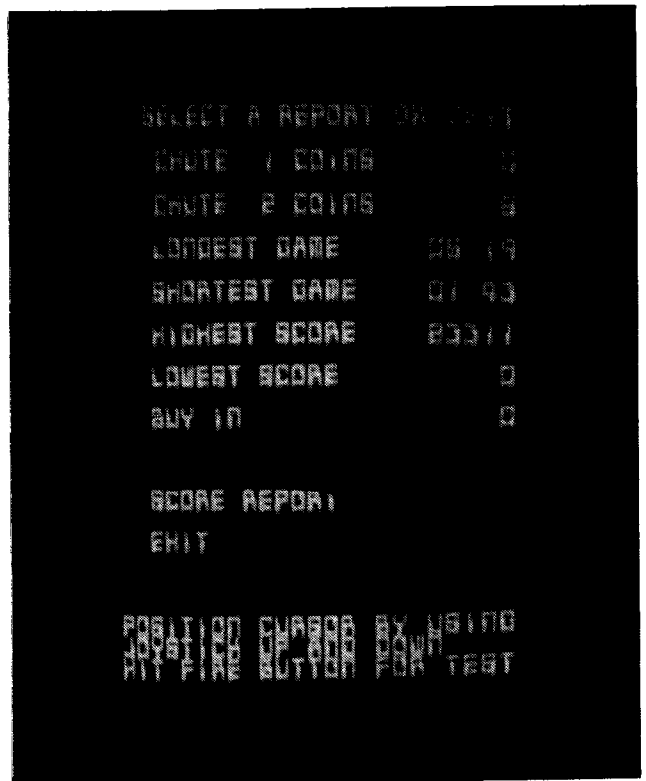


Figure 7 Self-Test—Bookkeeping

- In this category a basic bookkeeping function is performed. And with the selection of the "TIME REPORT" and the "SCORE REPORT", detailed breakdowns of game times and scores may be obtained.

In the TIME REPORT and SCORE REPORT sections of the BOOKKEEPING mode, the game will give displays which look like those shown in Figures 8 and 9 respectively.



Figure 8 Self-Test—Time Report

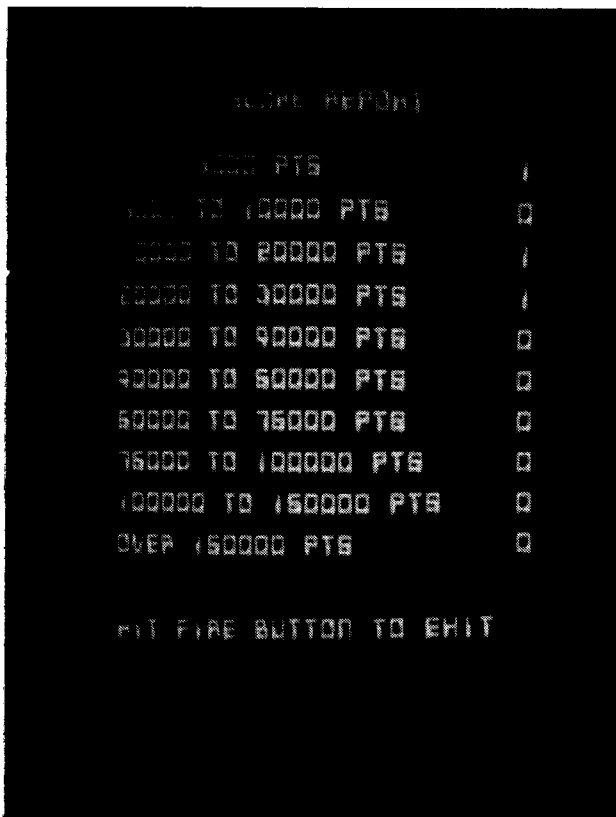
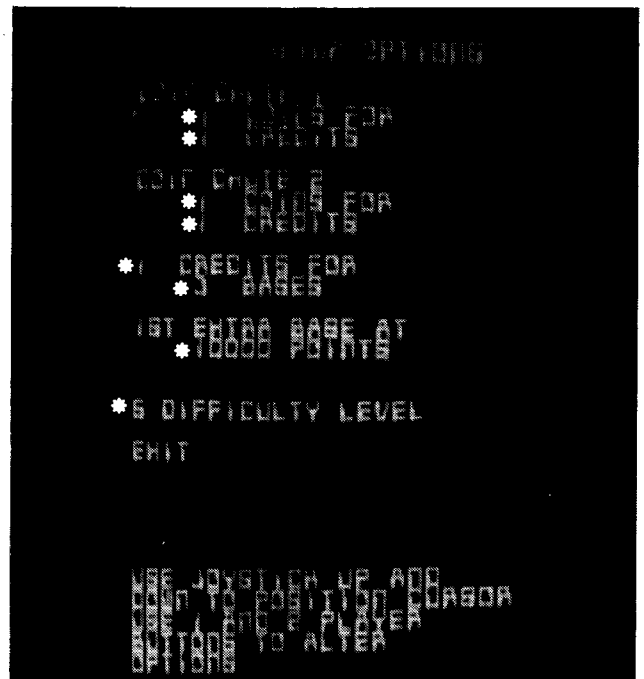


Figure 9 Self-Test—Score Report

During the SETUP OPTIONS section of the Self-Test mode, the game will give a display which looks like that shown in Figure 10.



\* = Factory recommended settings.

Figure 10 Self-Test—Setup Options

- In this category, all common game options may be changed from the control console: coins per credit, credits per base, bonus base(s) awarded at, difficulty level --, and so on.

The Difficulty Level setting has a range of 1 to 9 with 1 representing the easiest level of play and 9 representing the most difficult level of play. One is the factory recommended setting.

During the CHANNEL TEST section of the Self-Test mode, the game will give a display which looks like that shown in Figure 11.

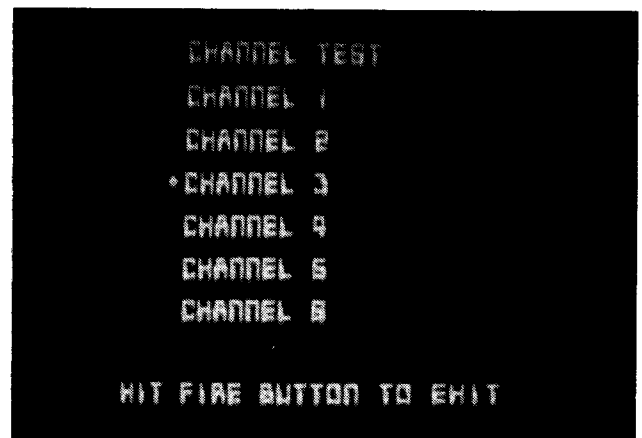


Figure 11 Self-Test—Channel Test

- In this category, the game conducts a test of its SOUND SYSTEM.

# A Glossary of Microprocessor Terms

**MICROPROCESSOR** — one or several microcircuits that perform the function of a computer's CPU. Sections of the circuit have arithmetic and comparative functions that perform computations and executive instructions.

**CPU** — central-processing unit. A computing system's "brain", whose arithmetic, control and logic elements direct functions and perform computations. The microprocessor section of a microcomputer is on one chip or several chips.

**PROM** — programmable read-only memory. User permanently sets binary on-off bits in each cell by selectively fusing or not fusing electrical links. Non-erasable. Used for low-volume applications.

**EPROM** — erasable, programmable, read-only memory. Can be erased by ultraviolet light bath, then reprogrammed. Frequently used during design and

development to get programs debugged, then replaced by ROM for mass production.

**ROM** — read-only memory. The program, or binary on-off bit pattern, is set into ROM during manufacture, usually as part of the last metal layer put onto the chip. Nonerasable. Typical ROM's contain up to 16,000 bits of data to serve as the microprocessor's basic instructions.

**RAM** — random-access memory. Stores binary bits as electrical charges in transistor memory cells. Can be read or modified through the CPU. Stores input instructions and results. Erased when power is turned off.

**LSI** — large scale integration. Formation of hundreds or thousands of so-called gate circuits on semiconductor chips. Very large scale integration (VLS) involves microcircuits with the greatest component density.

**MOS** — metal-oxide semiconductor. A layered construction technique for integrated circuits that achieves high component densities. Variations in MOS chip structures create circuits with speed and low-power requirements, or other advantages (static will damage a MOS chip).

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## Introduction to the Z-80 CPU

The term "microcomputer" has been used to describe virtually every type of small computing device designed within the last few years. This term has been applied to everything from simple "microprogrammed" controllers constructed out of TTL MSI up to low end minicomputers with a portion of the CPU constructed out of TTL LSI "bit slices." However, the major impact of the LSI technology within the last few years has been with MOS LSI. With this technology, it is possible to fabricate complete and very powerful computer systems with only a few MOS LSI components.

The Zilog Z-80 family of components can be configured with any type of standard semiconductor memory to generate computer systems with an extremely wide range of capabilities. For example, as few as two LSI circuits and three standard TTL MSI packages can be combined to form a simple controller. With additional memory and I/O devices a computer can be constructed with capabilities that only a minicomputer could previously deliver.

New products using the MOS LSI microcomputer are being developed at an extraordinary rate. The Zilog Z-80 component set has been designed to fit into this market through the following factors:

1. The Z-80 is fully software compatible with the popular 8080A CPU.
2. Existing designs can be easily converted to include the Z-80.
3. The Z-80 component set is at present superior in both software and hardware capabilities to any other microcomputer system on the market today.
4. For increased throughput the Z80A operating at a 4 MHz clock rate offers the user significant speed advantages.

Microcomputer systems are extremely simple to construct using Z-80 components. Any such system consists of three parts:

1. **CPU (Central Processing Unit)**
2. **Memory**
3. **Interface Circuits to peripheral devices**

The CPU is the heart of the system. Its function is to obtain instructions from the memory and perform the desired operations. The memory is used to contain instructions and in most cases data that is to be processed. For example, a typical instruction sequence may be to read data from a specific peripheral device, store it in a location in memory, check the parity and write it out to another peripheral device. Note that the Zilog component set includes the CPU and various general purpose I/O device controllers, while a wide range of memory devices may be used from any source. Thus, all required components can be connected together in a very simple manner with virtually no other external logic.



## General Purpose Registers

There are two matched sets of general purpose registers, each set containing six 8-bit registers that may be used individually as 8-bit registers or as 16-bit register pairs by the programmer. One set is called BC, DE and HL while the complementary set is called BC', DE' and HL'. At any one time the programmer can select either set of registers to work with through a single exchange command for the entire set. In systems where fast interrupt response is required, one set of general purpose registers and an accumulator/flag register may be reserved for handling this very fast routine. Only a simple exchange command need be executed to go between the routines. This greatly reduces interrupt service time by eliminating the requirement for saving and retrieving register contents in the external stack during interrupt or subroutine processing. These general purpose registers are used for a wide range of applications by the programmer. They also simplify programming, especially in ROM based systems where little external read/write memory is available.

## Arithmetic & Logic Unit (ALU)

The 8-bit arithmetic and logical instructions of the CPU are executed in the ALU. Internally the ALU communicates with the registers and the external

data bus on the internal data bus. The type of functions performed by the ALU include:

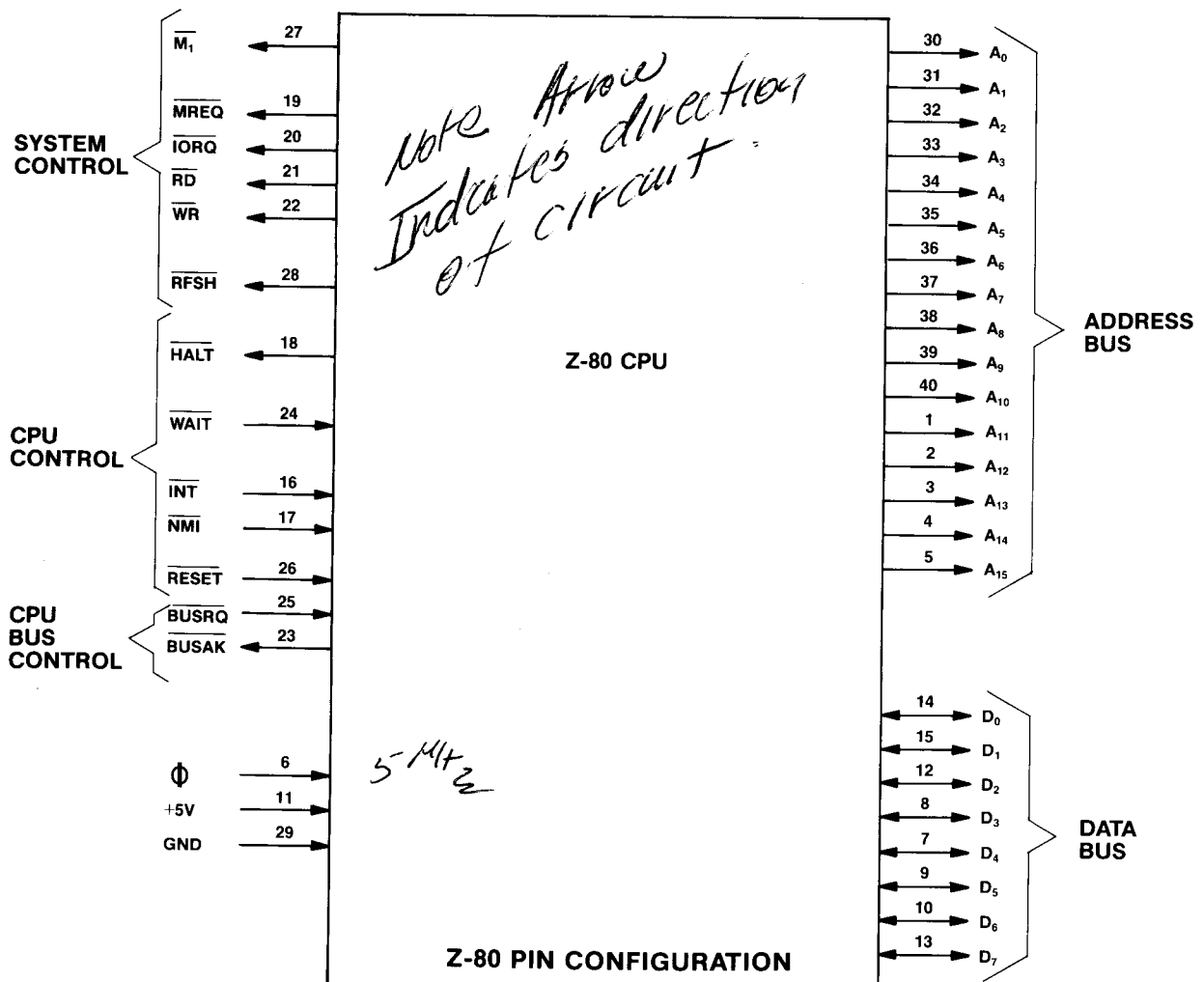
<b>Add</b>	Left or right shifts or rotates (arithmetic and logical)
<b>Subtract</b>	Increment
<b>Logical AND</b>	Decrement
<b>Logical OR</b>	Set bit
<b>Logical Exclusive OR</b>	Reset bit
<b>Compare</b>	Test bit

## Instruction Register and CPU Control

As each instruction is fetched from memory, it is placed in the instruction register and decoded. The control sections performs this function and then generates and supplies all of the control signals necessary to read or write data from or to the registers, control the ALU and provide all required external control signals.

## Z-80 CPU Pin Description

The Z-80 CPU is packaged in an industry standard 40 pin Dual In-Line Package. The I/O pins are shown in the below figure and the function of each is described.



**A<sub>0</sub>-A<sub>15</sub>**  
**(Address Bus)**

Tri-state output, active high. A<sub>0</sub>-A<sub>15</sub> constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the 8 lower address bits to allow the user to directly select up to 256 input or 256 output ports. A<sub>0</sub> is the least significant address bit. During refresh time, the lower 7 bits contain a valid refresh address.

**D<sub>0</sub>-D<sub>7</sub>**  
**(Data Bus)**

Tri-state input/output, active high. D<sub>0</sub>-D<sub>7</sub> constitute an 8-bit bidirectional data bus. The data bus is used for data exchanges with memory and I/O devices.

**M<sub>1</sub>**  
**(Machine Cycle one)**

Output, active low. M<sub>1</sub> indicates that the current machine cycle is the OP code fetch cycle of an instruction execution. Note that during execution of 2-byte op-codes, M<sub>1</sub> is generated as each op code byte is fetched. These two byte op-codes always begin with CBH, DDH, EDH or FDH. M<sub>1</sub> also occurs with IORQ to indicate an interrupt acknowledge cycle.

**MREQ**  
**(Memory Request)**

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

**IORQ**  
**(Input/Output Request)**

Tri-state output, active low. The IORQ signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An IORQ signal is also generated with an M<sub>1</sub> signal when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during M<sub>1</sub> time while I/O operations never occur during M<sub>1</sub> time.

**RD**  
**(Memory Read)**

Tri-state output, active low. RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

**WR**  
**(Memory Write)**

Tri-state output, active low. WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

**RFSH**  
**(Refresh)**

Output, active low. RFSH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current MREQ signal should be used to do a refresh read to all dynamic memories.

**HALT**  
**(Halt state)**

Output, active low. HALT indicates that the CPU has executed a HALT software instruction and is awaiting either a non maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

**WAIT**  
**(Wait)**

Input, active low. WAIT indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. This signal allows memory or I/O devices of any speed to be synchronized to the CPU.

**INT**  
**(Interrupt Request)**

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (IORQ during M<sub>1</sub> time) is sent out at the beginning of the next instruction cycle. The CPU can respond to an interrupt in three different modes that are described in detail in section 5.4 (CPU Control Instructions).

**NMI**  
**(Non-Maskable Interrupt)**

Input, negative edge triggered. The non maskable interrupt request line has a higher priority than INT and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. NMI automatically forces the Z-80 CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycles can prevent the current instruction from ending, and that a BUSRQ will override a NMI.

**RESET**

Input, active low. RESET forces the program counter to zero and initializes the CPU. The CPU initialization includes:

- 1) Disable the interrupt enable flip-flop

- 2) Set Register I = 00H
- 3) Set Register R = 00H
- 4) Set Interrupt Mode 0

During reset time, the address bus and data bus go to a high impedance state and all control output signals go to the inactive state.

#### **BUSRQ**

##### **(Bus Request)**

Input, active low. The bus request signal is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these buses. When BUSRQ is activated, the CPU will set these

buses to a high impedance state as soon as the current CPU machine cycle is terminated.

#### **BUSAK**

##### **(Bus Acknowledge)**

Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.

#### **CLK**

##### **(Clock)**

Single phase TTL level clock which requires only a 330 ohm pull-up resistor to +5 volts to meet all clock requirements.

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## MCR II SYSTEM P.C. BOARD JUMPER OPTIONS

### VIDEO GENERATOR P.C. BOARD

MANUFACTURER	EPROM NO.	JW#1	JW#2	JW#3	JW#4	JW#5	JW#6	JW#7	JW#8
MOTOROLA	68764	#	* <i>CUT</i>	*	#	*	*	*	*
	68766	#	*	*	#	*	*	*	*
INTEL	2764	*	#	#	*	#	*	*	#
T. I.	2564	#	*	*	#	*	#	#	*

### SUPER C.P.U. P.C. BOARD

#### JUMPER OPTIONS FOR PROGRAM ROMS ONLY

MANUFACTURER	EPROM NO.	JW#2	JW#4	JW#5	JW#6	JW#7	JW#18	JW#19	
MOTOROLA	68764	#	#	*	#	*	*	#	
	68766	#	#	*	#	*	*	#	
T. I.	2564	#	#	*	#	*	*	#	
INTEL	2764	*	*	#	*	#	#	*	

#### JUMPER OPTIONS FOR BACKGROUND ROMS ONLY

MANUFACTURER	EPROM NO.	JW#10	JW#11	JW#12	JW#13	JW#14	JW#15	JW#16	JW#17
MOTOROLA	68764	*	#	*	#	*	#	#	*
	68766	*	#	*	#	*	#	#	*
T. I.	2564	*	#	*	#	*	#	#	*
INTEL	2764	#	*	#	*	#	*	*	#

### SOUND I/O P. C. BOARD

MANUFACTURER	EPROM NO.	JW#1	JW#2	
NUMEROUS MFR'S	2532	*	#	
NUMEROUS MFR'S	2732	#	*	

\* = CUT JUMPER WIRES WHERE THIS SYMBOL "\*" APPEARS.

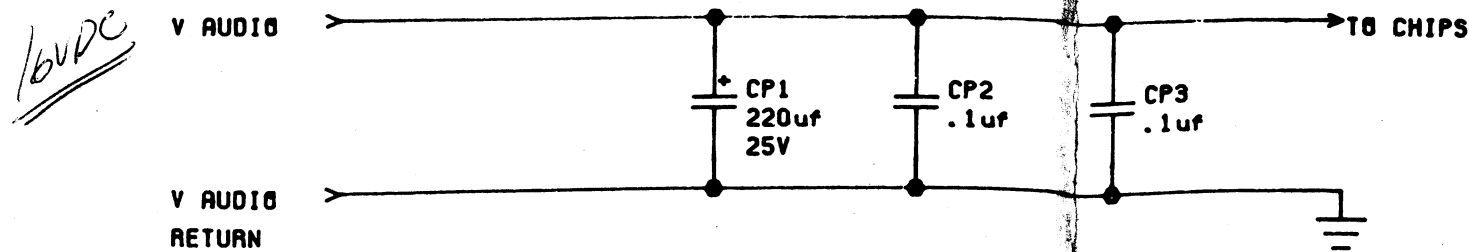
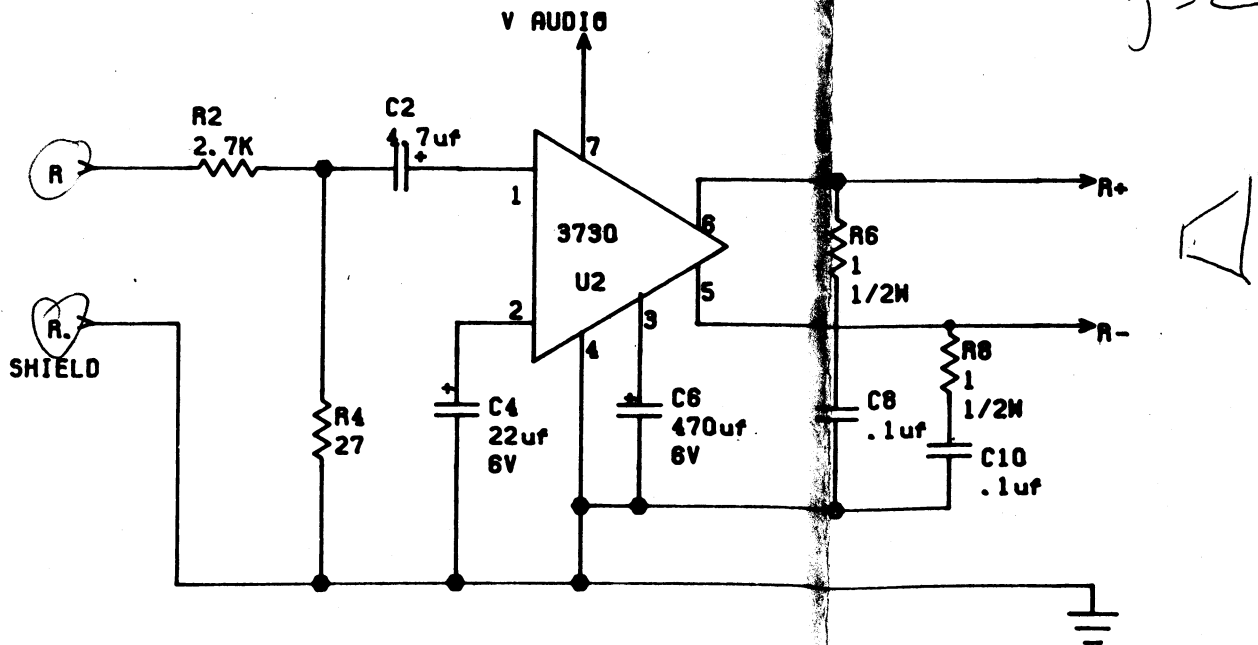
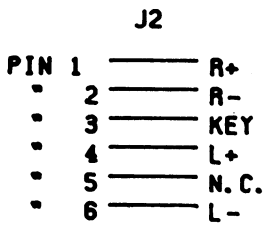
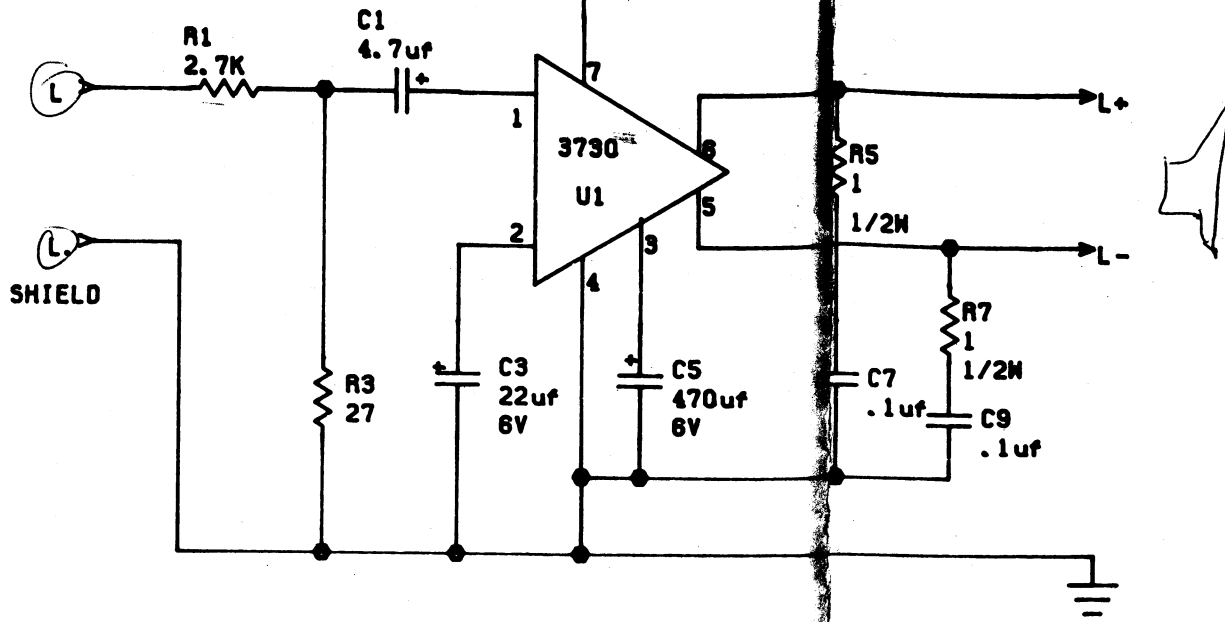
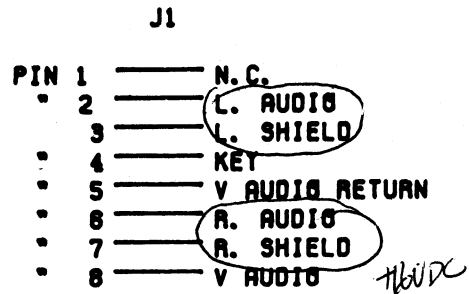
# = LEAVE JUMPER WIRES IN WHERE THIS SYMBOL "#" APPEARS.

The above table illustrates the fact that the Video Generator P.C. Board used in the MCR II System has 8 jumper wires, the SUPER C.P.U. P.C. Board used in the MCR II System has 19 jumper wires, and the Sound I/O P.C. Board used in the MCR II System has 2 jumper wires.

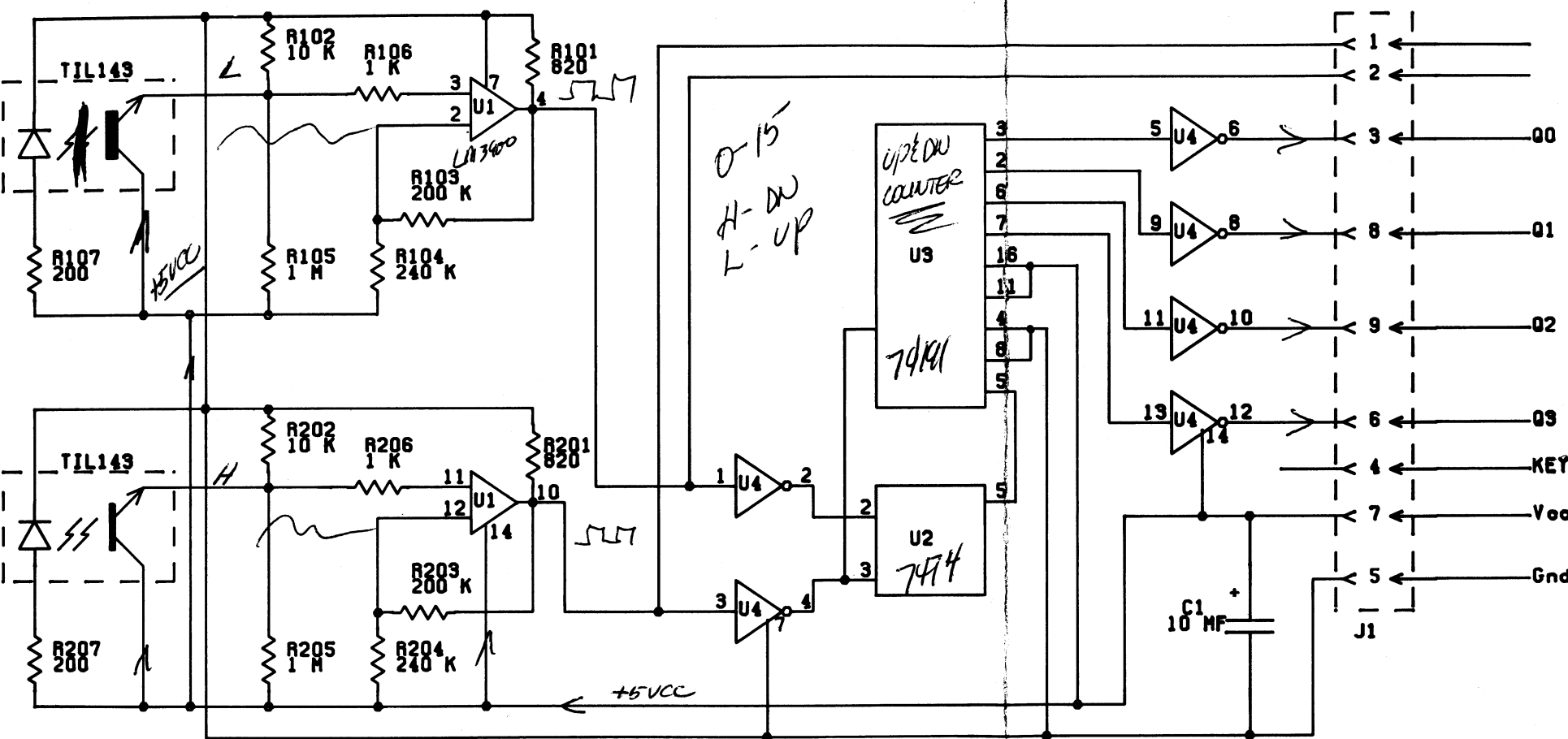
All of the above Boards can be used with a variety of different **SETS of EPROM chips**. However, these EPROMS are not all made by the same manufacturer

and do have some internal differences. So, in order to make them function properly in their respective P.C. Boards, certain jumper wires on these Boards have to be cut.

The above table tells you which jumpers to cut (depending on which EPROM set you're going to use) by showing a "\*" under that jumper wire's number. If there is **NO** "\*" under a jumper wire's number, **THAT PARTICULAR JUMPER WIRE IS NOT TO BE CUT.**



REVISIONS	
<b>MIDWAY MFG. CO.</b>	
FRANKLIN PK. ILL.	
PART NO. M051-00986-E011	
USED ON TRON	NO. REQ'D 1 PER.
SCALE NONE	SCHEMATIC, DUAL POWER AMP,
HEAT TREAT	A082-90910-E000
MAT'L.	
FINISH	
DO NOT SCALE DWG.	DRN. <i>SKL</i>
DIM. TOLERANCES UNLESS SPECIFIED	CKD.
CONCENTRICITY T I R .003	
FRACTIONAL . . . . . 1/64	
DECIMAL . . . . . 005	
HOLE DIA . . . . . + .002 .000	DATE 5/17/82



0-15  
H-DU  
L-UP

1E0 Bd

- NOTES  
 U1-LM3900  
 U2-7474  
 U3-74191  
 U4-7414

PROJECT ENG: C.MEDNICK

CKD.	DO NOT SCALE DWG.		REVISIONS
DRN. TJK	DATE 8/26/81	USED ON	MIDWAY MFG. CO. FRANKLIN PK. ILL.
heat treat	scale FULL	NO. REQ'D 1 PER	
mat'L	BINARY ANGLE DECODER SCHEMATIC A082-91391-C000		PART NO.
finish			M051-00968-C004

Chip Number	Function
MB8416	Ram 2K x 8
6116LP-4	Ram 2K x 8
9860-07AXN-AXHD	PROM 82S123 (SB2-A)
Z-80 CTC	Counter timer circuit
0066-313BX-XXQX (MMC01)	H-T generator - custom
0066-314BX-XXQX (MMC02)	V-T generator - custom
0066-315BX-XXQX (MMC03)	Misc. V & H circuits - custom
0066-316BX-XXQX (MMC06)	Misc. TTL circuits - custom
0066-322BX-XXQX (MMC04)	NVR controller - custom
AY-3-8910 (8910)	Sound generator
LM3900	Quad operational amplifier
MC3403	Quad operational amplifier

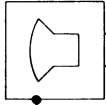
#### Misc. Components

16.00 & 19.9 MHZ	Z-TAL
2N4123	Transistor NPN
2N4403	Transistor PNP
MPSA70	Transistor PNP
TIP110	Transistor NPN

#### Logic Boards Integrated Circuits

Chip Number	Function
7400	Quad 2 input Nand
74LS02	Quad 2 input Nor
74LS04	Hex inverter
7406	Hex inverter open collector
7407	Hex buffer open collector
74LS08	Quad 2 input And
74LS20	Dual 4 input Nand
7427	Triple 3 input Nor
74LS30	8 input Nand
74LS32	Quad 2 input Or
74LS74	Dual "D" Flip-Flop
74LS86	Quad 2 input exclusive Or
7489	64 bit ram 16 x 4
74126	Quad buffer tri-state
74LS138	3 to 8 line decoder
74LS153	Dual 4 to 1 line multiplexer
74LS155	Dual 2 to 4 line decoder
74LS157	Quad 2 to 1 line multiplexer
74160	4 bit decade counter
74161	4 bit binary counter
74166	8 bit shift register
74LS174	Hex "D" Flip-Flop
74175	Quad "D" Flip-Flop
74LS191	Up/down binary counter
74LS194	8 bit shift register
74LS244	Octal buffer tri-state
74LS245	Octal buss transceiver
74LS273	Octal "D" Flip-Flop
74LS283	4 bit full adder
74LS367	Hex buss driver
74LS374	Octal "D" Flip-Flop tri-state
74LS670	4 x 4 register files
4017	Decade counter/divider
14016	Quad analog switch
14024	7 stage ripple counter
14053	Triple 2 channel analog multiplexer
Z80	CPU 2.5 MHz
Z80A	CPU 4 MHz
D780C	CPU 2.5 MHz
D780C-1	CPU 4 MHz
TMS2564	8K x 8 EPROM
MBM2732	4K x 8 EPROM
HN462532	4K x 8 EPROM
2114	Ram 1K x 4
93422	Ram 256 x 4
M58725	Ram 2K x 8
4801AN-90	Ram 1K x 8
4118A-4	Ram 1K x 8
93419 or 82S09	64 X 9 Color Ram
74LS133	13 input Nand Gate

VIDEO MONITOR



FLUORESCENT LIGHT

FAN

VOLTAGE SELECTOR

125VA

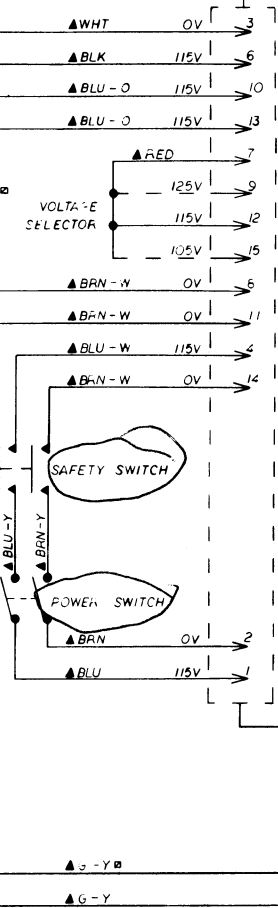
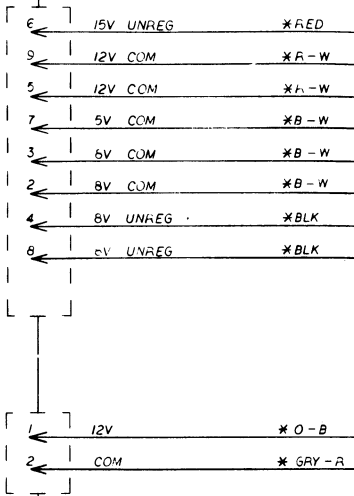
FCC

CONN 3 15 POS POWER CHASSIS A945-00020-0000

CONN 1 9 POS

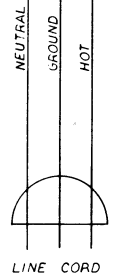
CONN 4 2 POS

CONN 2 3 POS



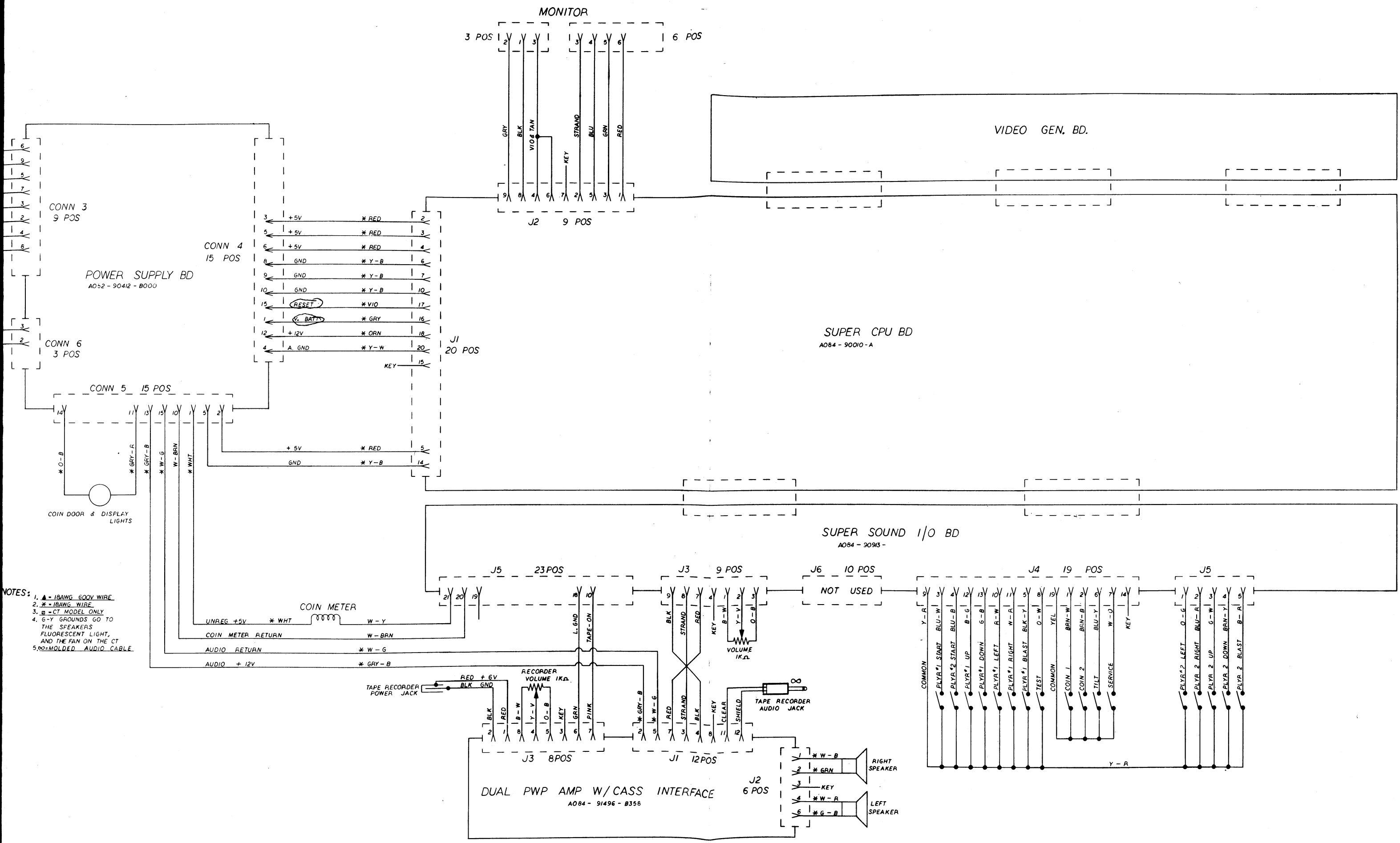
- YELLOW GND STRAP TO MONITOR
- YELLOW GND STRAP TO COIN DIAL
- YELLOW GND STRAP TO LOGIC CARD RACK
- YELLOW GND STRAP TO CONTROL

REVISION	DATE	NAME



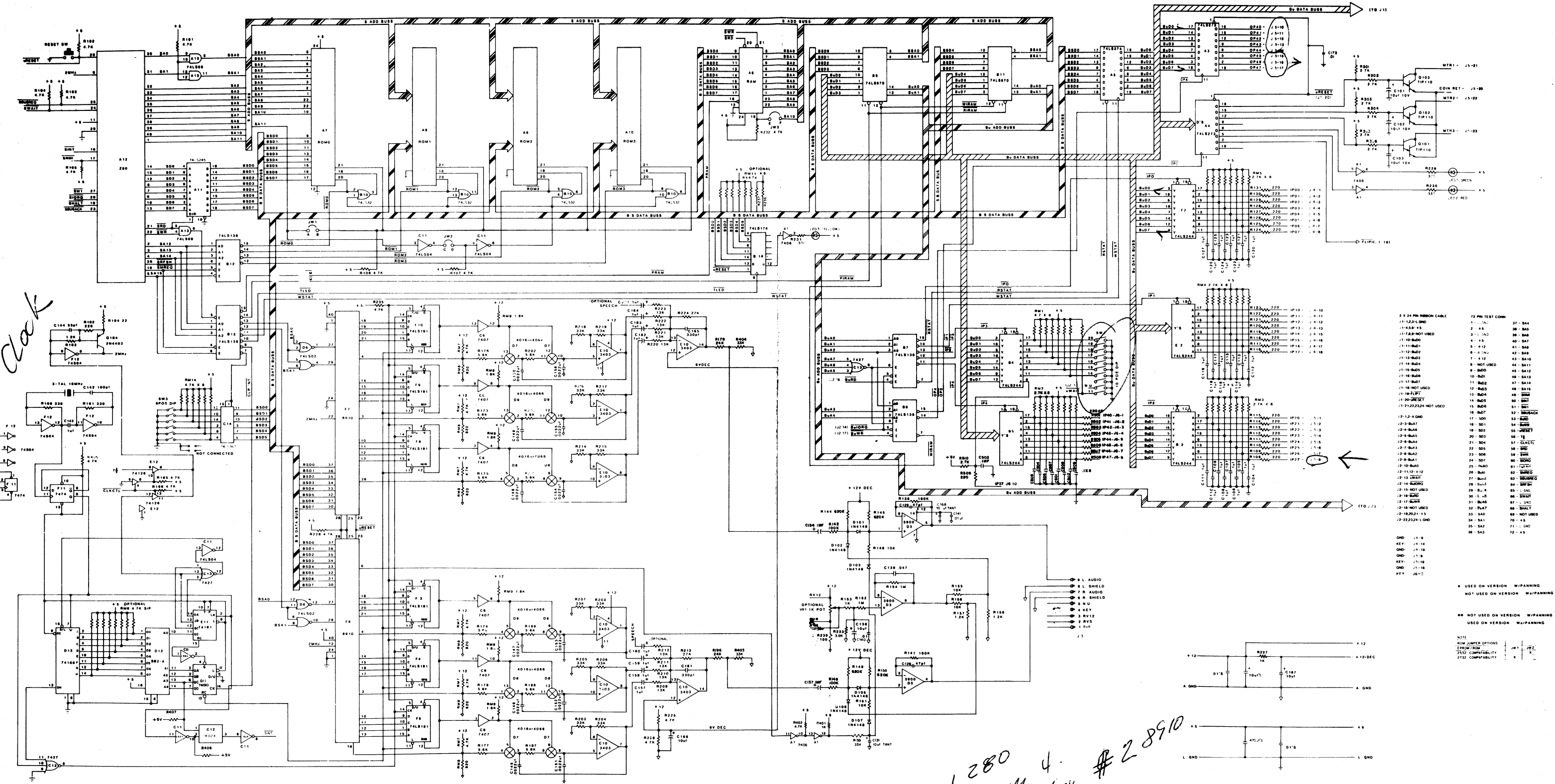
JOURNEY  
 M051-00358-A003  
**Bally** / MIDWAY  
 10601 W BELMONT  
 FRANKLIN PARK, ILL. 60131





- NOTES:
- ▲ - 18AWG 600V WIRE
  - \* - 18AWG WIRE
  - - CT MODEL ONLY
  - - Y GROUNDS GO TO THE SPEAKERS FLUORESCENT LIGHT, AND THE FAN ON THE CT
  - 5.00" MOLDED AUDIO CABLE

clock

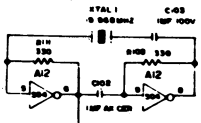


Sound.  
160 ports.  
DIP SW.

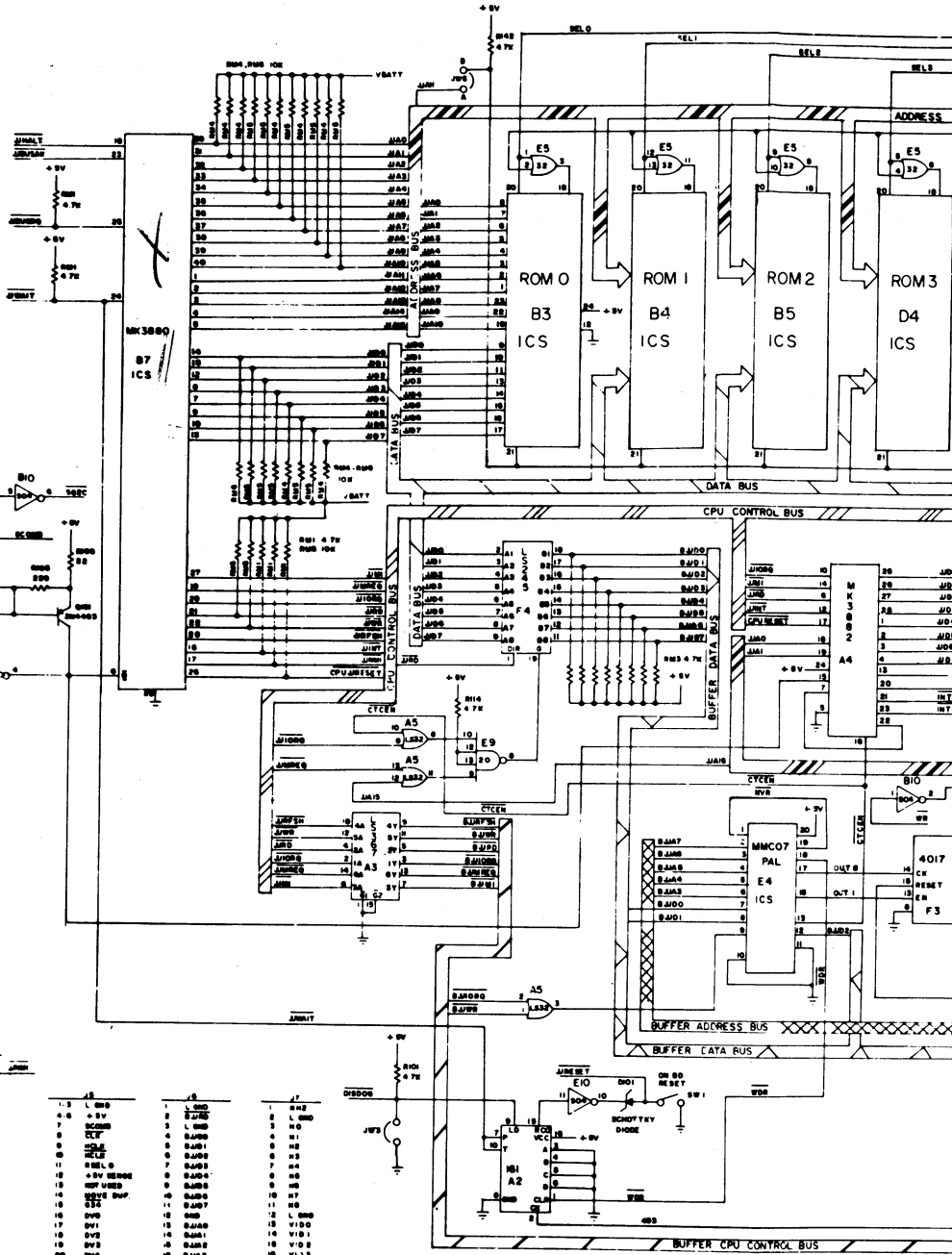
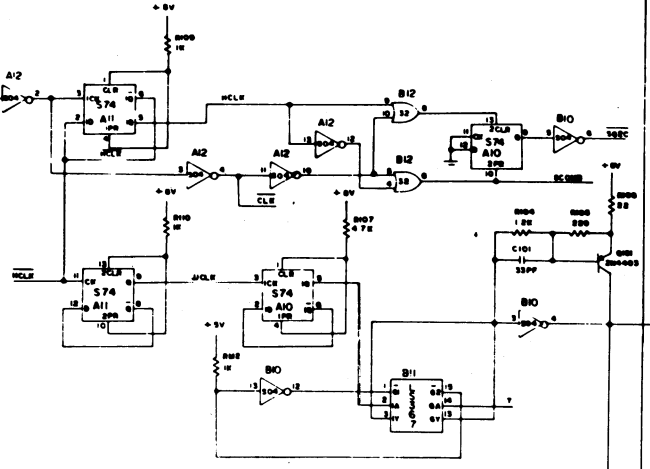
1. 280  
2. Rom 4.  
3. Sound ber # 28910  
4. AG RAM  
5. Buffer. 160-  
6. Transistor output-

NO.	DESCRIPTION	QTY.	PER
1	280	1	1
2	ROM 4	4	1
3	SOUND BER # 28910	1	1
4	AG RAM	1	1
5	BUFFER 160-	1	1
6	TRANSISTOR OUTPUT	1	1

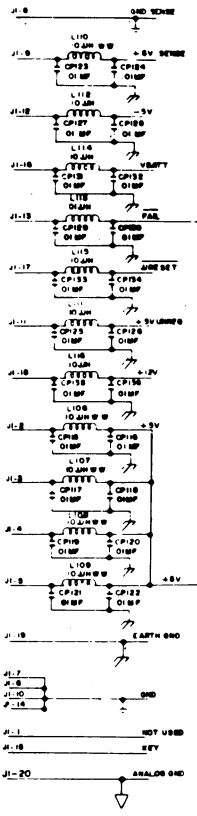
MIDWAY MFG. CO.  
SCHEMATIC DRAWING  
SUPER SOUND I/O  
A094-30813-EG00  
M051-00628-A014



*Clock*



13	14
1 L 0.00	1 A 0.00
2 L 0.00	2 A 0.00
3 L 0.00	3 BAA7
4 +5V	4 BAA6
5 +5V	5 BAA5
6 +5V	6 BAA4
7 NOT USED	7 BAA3
8 NOT USED	8 BAA2
9 NOT USED	9 BAA1
10 BAA0	10 BAA0
11 BAA1	11 +5V
12 BAA2	12 +5V
13 BAA3	13 BAA7
14 BAA4	14 BAA6
15 BAA5	15 NOT USED
16 BAA6	16 BAA5
17 BAA7	17 BAA4
18 NOT USED	18 NOT USED
19 FLIP	19 +5V
20 BAA0	20 +5V
21 NOT USED	21 +5V
22 NOT USED	22 L 0.00
23 NOT USED	23 L 0.00
24 NOT USED	24 L 0.00

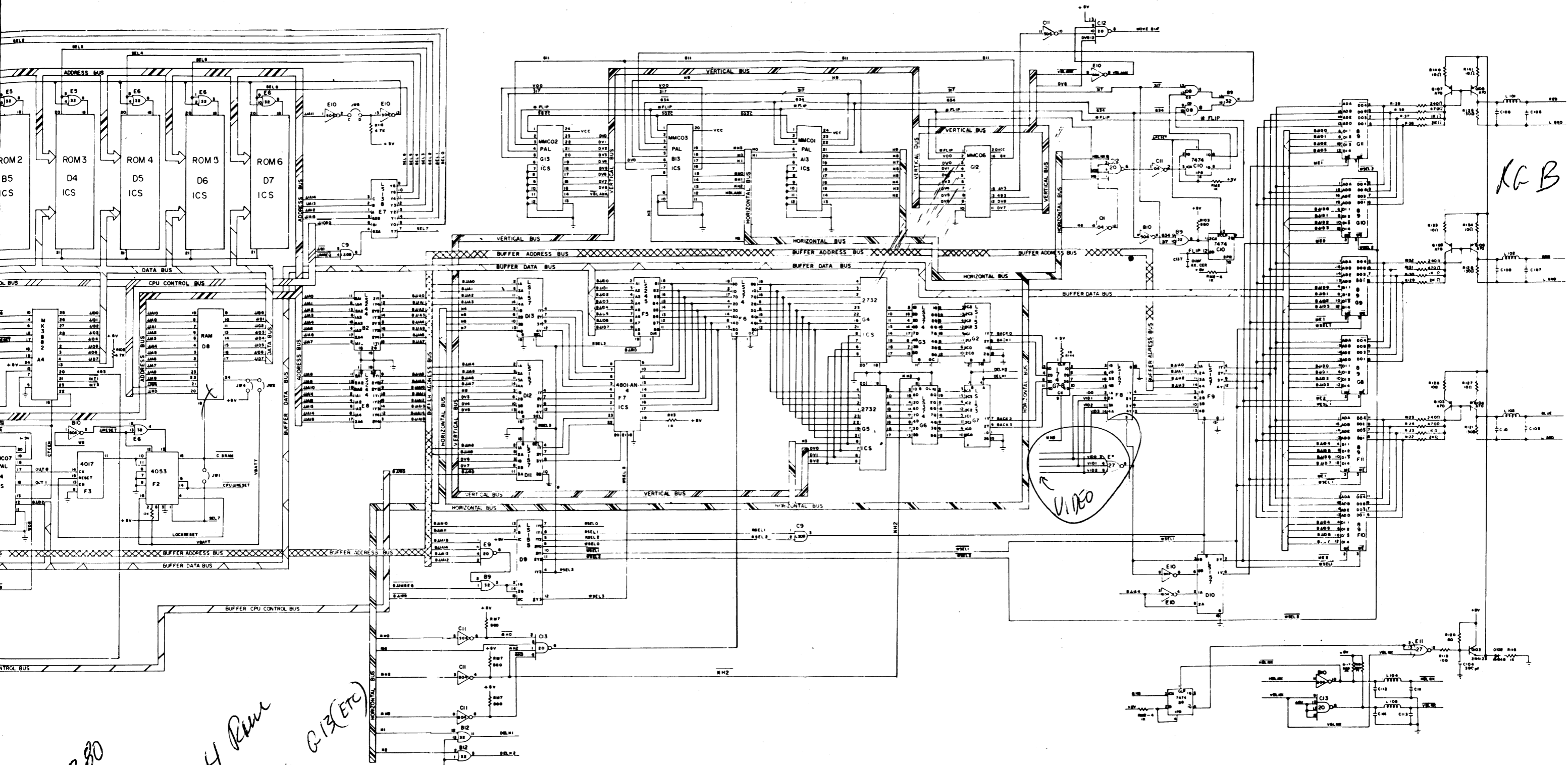


15	16	17
1 L 0.00	1 L 0.00	1 R12
2 +5V	2 L 0.00	2 R10
3 BAA7	3 BAA6	3 R11
4 CLE	4 BAA5	4 R1
5 BAA6	5 BAA4	5 R2
6 BAA5	6 BAA3	6 R3
7 BAA4	7 BAA2	7 R4
8 BAA3	8 BAA1	8 R5
9 BAA2	9 BAA0	9 R6
10 BAA1	10 BAA0	10 R7
11 BAA0	11 BAA0	11 R8
12 BAA7	12 BAA6	12 L 0.00
13 BAA6	13 BAA5	13 VDD
14 BAA5	14 BAA4	14 VDD
15 BAA4	15 BAA3	15 VDD
16 BAA3	16 BAA2	16 VDD
17 BAA2	17 BAA1	17 VDD
18 BAA1	18 BAA0	18 VDD
19 BAA0	19 BAA0	19 VDD
20 BAA0	20 BAA0	20 VDD
21 BAA0	21 BAA0	21 VDD
22 BAA0	22 BAA0	22 +5V
23 BAA0	23 BAA0	23 L 0.00
24 BAA0	24 BAA0	24 R9

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100															
REC	L 0.00	SP	ADJ006	ADJ007	ADJ008	ADJ009	ADJ010	ADJ011	ADJ012	ADJ013	ADJ014	ADJ015	ADJ016	ADJ017	ADJ018	ADJ019	ADJ020	ADJ021	ADJ022	ADJ023	ADJ024	ADJ025	ADJ026	ADJ027	ADJ028	ADJ029	ADJ030	ADJ031	ADJ032	ADJ033	ADJ034	ADJ035	ADJ036	ADJ037	ADJ038	ADJ039	ADJ040	ADJ041	ADJ042	ADJ043	ADJ044	ADJ045	ADJ046	ADJ047	ADJ048	ADJ049	ADJ050	ADJ051	ADJ052	ADJ053	ADJ054	ADJ055	ADJ056	ADJ057	ADJ058	ADJ059	ADJ060	ADJ061	ADJ062	ADJ063	ADJ064	ADJ065	ADJ066	ADJ067	ADJ068	ADJ069	ADJ070	ADJ071	ADJ072	ADJ073	ADJ074	ADJ075	ADJ076	ADJ077	ADJ078	ADJ079	ADJ080	ADJ081	ADJ082	ADJ083	ADJ084	ADJ085	ADJ086	ADJ087	ADJ088	ADJ089	ADJ090	ADJ091	ADJ092	ADJ093	ADJ094	ADJ095	ADJ096	ADJ097	ADJ098	ADJ099	ADJ100

NOTES  
A - ANALOG  
E - EARTH  
L - LOGIC

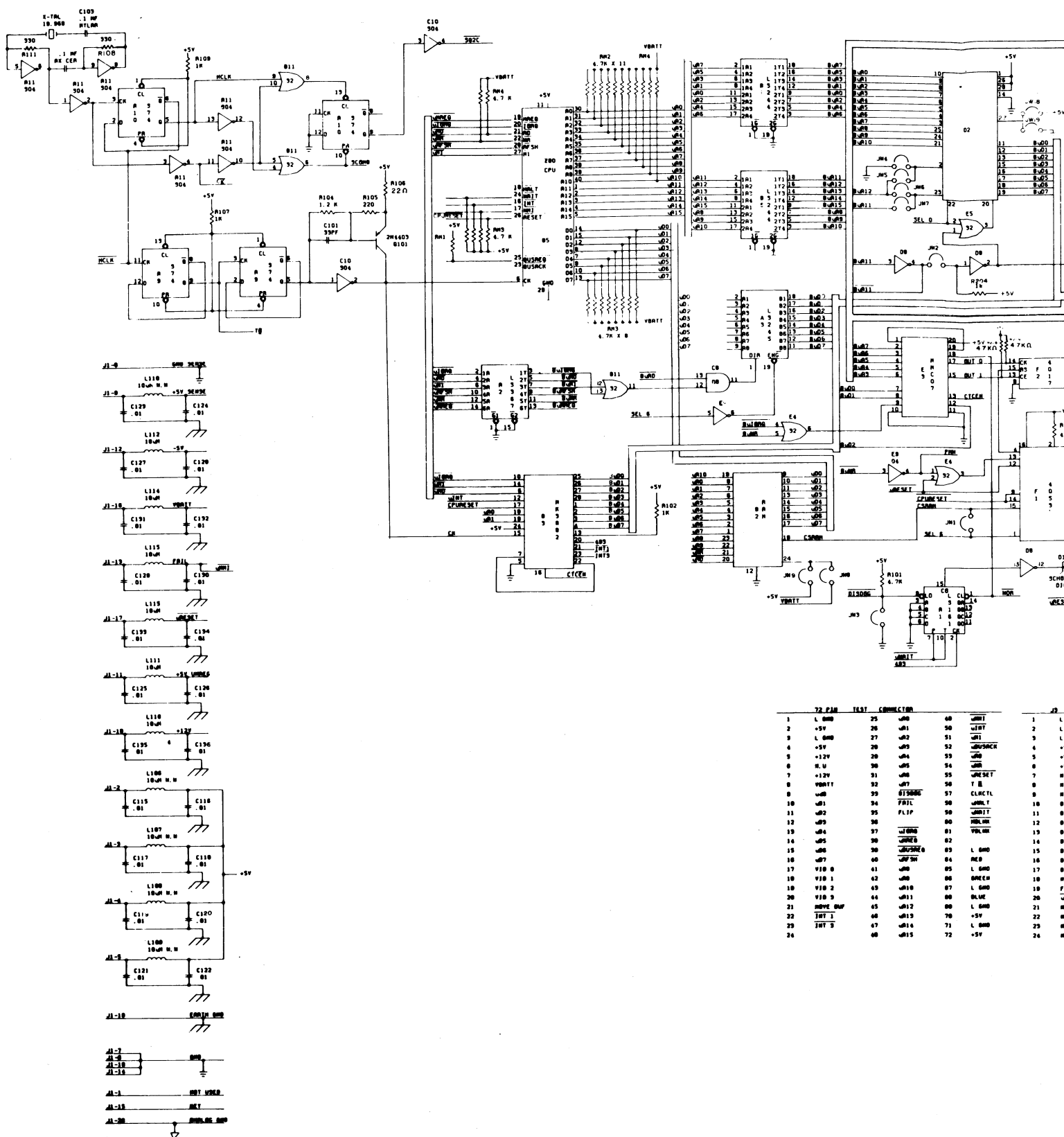
1-280  
2



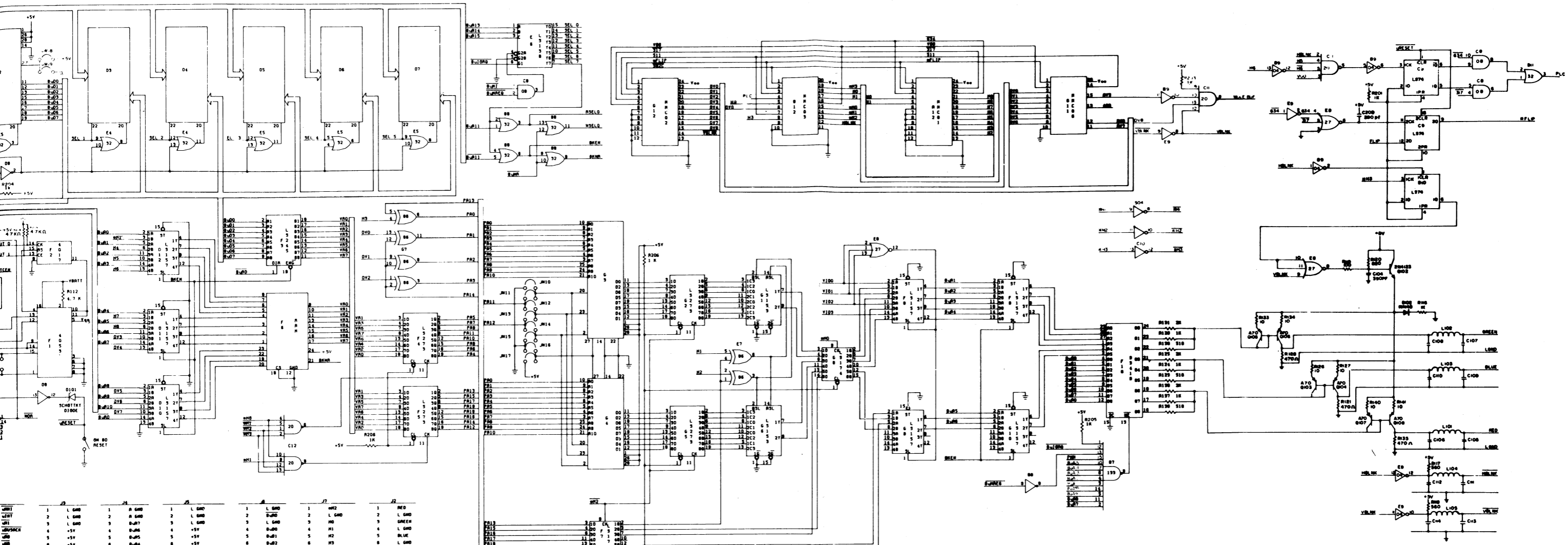
KGB

1 280  
 2 Kour  
 3 D 8 Buff Ram  
 4 Clock Chips G-13(ETC)  
 5 B.6 Ram  
 6 B.6 Ram F-7  
 7 Color Ram  
 7489  
 DFL 4CPU  
 Belt. 3CPU

PROJECT NO. 1	REVISION	DATE	DESIGNED BY	CHECKED BY
10/15/78	1	10/15/78		
CPU SCHEMATIC			MIDWAY MFG. CO.	
A082-80008-1000			MOS'00982-A006	



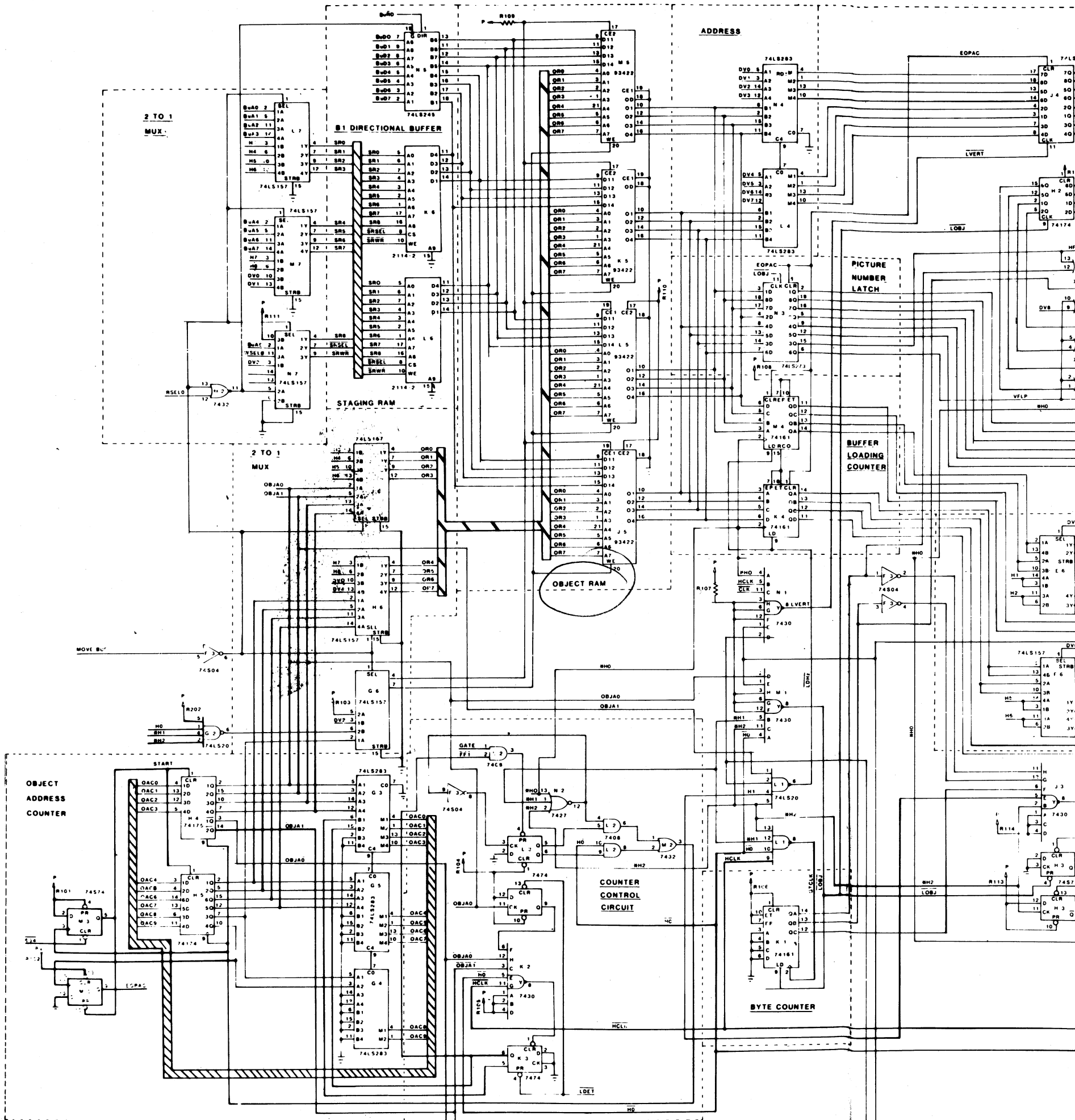
72	PIN	TEST	CONNECTION	J2	
1	L 000	25	U00	60	U00T
2	+5V	26	U01	50	U01T
3	L 000	27	U02	51	U02T
4	+5V	28	U03	52	U03PULSE
5	+12V	29	U04	53	U04
6	H.U	30	U05	54	U05
7	+12V	31	U06	55	U06SET
8	V00T1	32	U07	56	T E
9	U00	33	U08	57	CLK CTL
10	U01	34	U09	58	U01T
11	U02	35	U10	59	U02T
12	U03	36	U11	60	U03T
13	U04	37	U12	61	VOL SW
14	U05	38	U13	62	U05
15	U06	39	U14	63	L 000
16	U07	40	U15	64	U07
17	V10 0	41	U16	65	L 000
18	V10 1	42	U17	66	U08
19	V10 2	43	U18	67	L 000
20	V10 3	44	U19	68	BLUE
21	U08	45	U20	69	L 000
22	THT T	46	U21	70	+5V
23	THT S	47	U22	71	L 000
24		48	U23	72	+5V



NO.	SYMBOL	VALUE	NO.	SYMBOL	VALUE	NO.	SYMBOL	VALUE
1	L GND		1	L GND		1	RED	
2	L GND		2	L GND		2	L GND	
3	L GND		3	L GND		3	GREEN	
4	+5V		4	+5V		4	L GND	
5	+5V		5	+5V		5	H2	
6	+5V		6	+5V		6	H3	
7	H.U.		7	SCHEM		7	H4	
8	H.U.		8	CLR		8	H5	
9	H.U.		9	HCLR		9	H6	
10	H.U.		10	HCLR		10	H7	
11	+12V		11	HSEL0		11	H8	
12	+12V		12	+5V DEWSE		12	L GND	
13	H.U.		13	H.U.		13	V10 0	
14	H.U.		14	H.U.		14	V10 1	
15	H.U.		15	H.U.		15	V10 2	
16	H.U.		16	H.U.		16	V10 3	
17	H.U.		17	H.U.		17	HSEL 0	
18	H.U.		18	H.U.		18	L GND	
19	PLIP		19	+5V		19	H.U.	
20	BLNK		20	+5V		20	H.U.	
21	L GND		21	H.U.		21	H.U.	
22	+5V		22	L GND		22	L GND	
23	L GND		23	H.U.		23	H.U.	
24	+5V		24	L GND		24	L GND	

NOTES  
 H.U. = HUMAN USED  
 E = EARTH  
 L = LOGIC  
 H.U. = NOT USED

PROJECT ENG. A. GHOSH		MIDWAY MFG. CO.	
DATE: 06/22/82	SCALE: 1:1	FULL	PER
SUPER CPU SCHEMATIC DRAWING		A082-90010-C000	
MOSI-00628-A008			



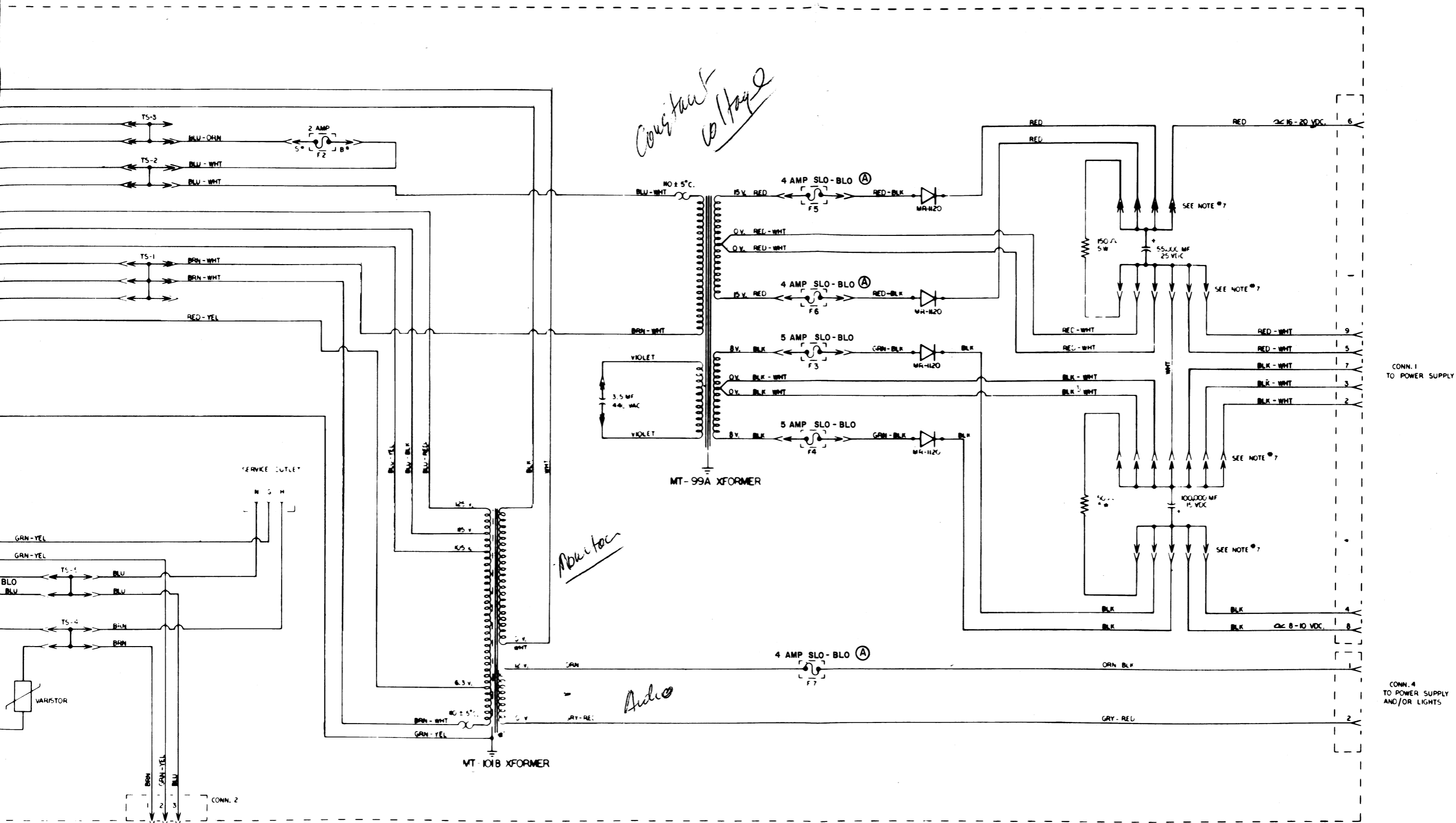












*Constant Voltage*

*Audio*

*Audio*

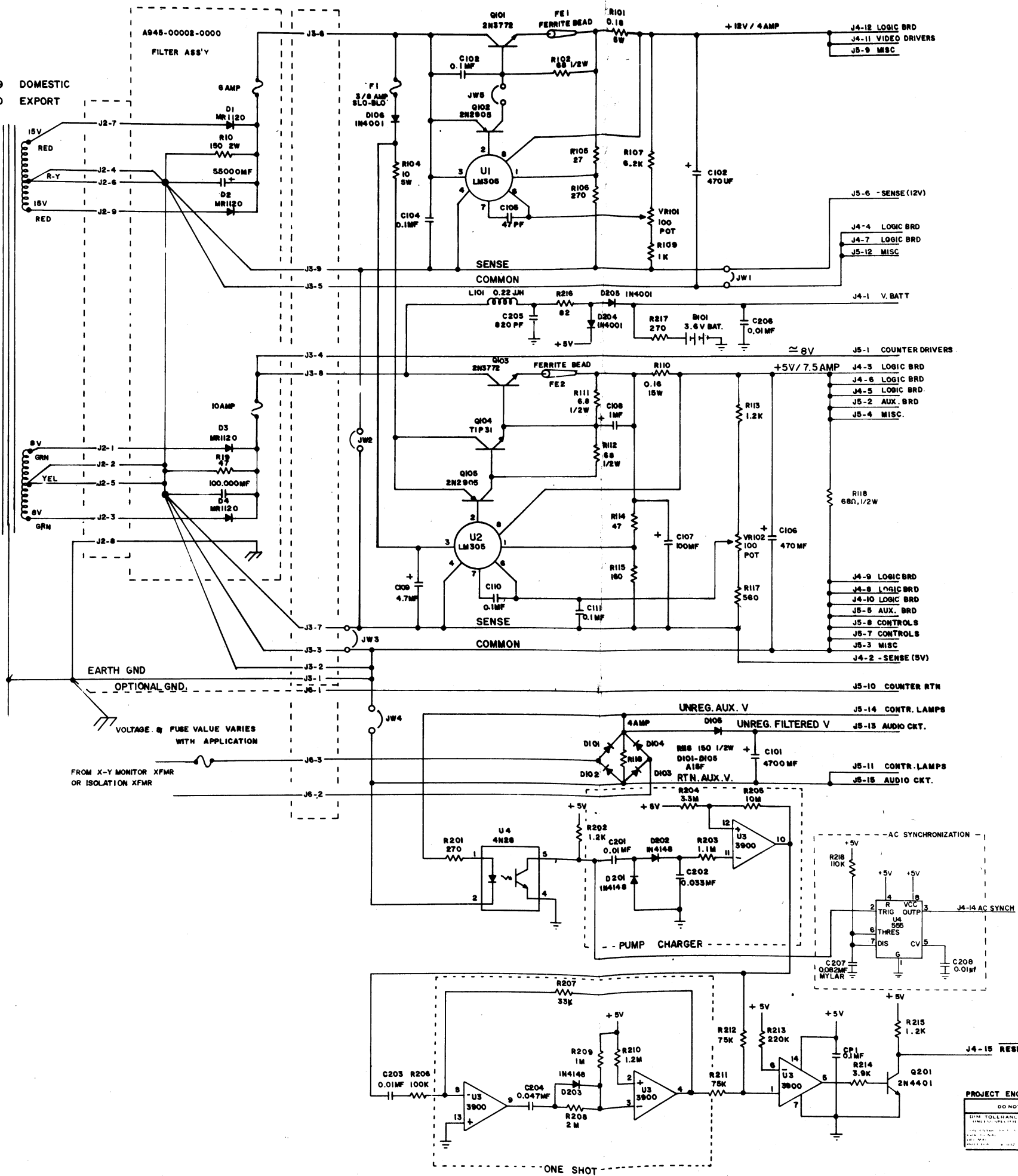
- NOTES:
1. A\* - WHEN USED
  2. B\* - BOTTOM TERMINAL
  3. S\* - SIDE TERMINAL
  4. TS1-5 - TERMINAL BARRIER STRIP POSITIONS
  5. + - CHASSIS EARTH GND.
  6. (---) - ALTERNATE COLOR
  7. TERMINATION ON CAPACITOR POST
  8. NOT AVAILABLE ON MT-101A

POWER CHASSIS \*125 VA  
 115V. - 60Hz.  
 PART NO. A945-00020-0000  
 DWG. NO. M051-00945-B037

BALLY / MIDWAY  
 10601 W. BELMONT AVE.  
 FRANKLIN PARK, IL. 60131

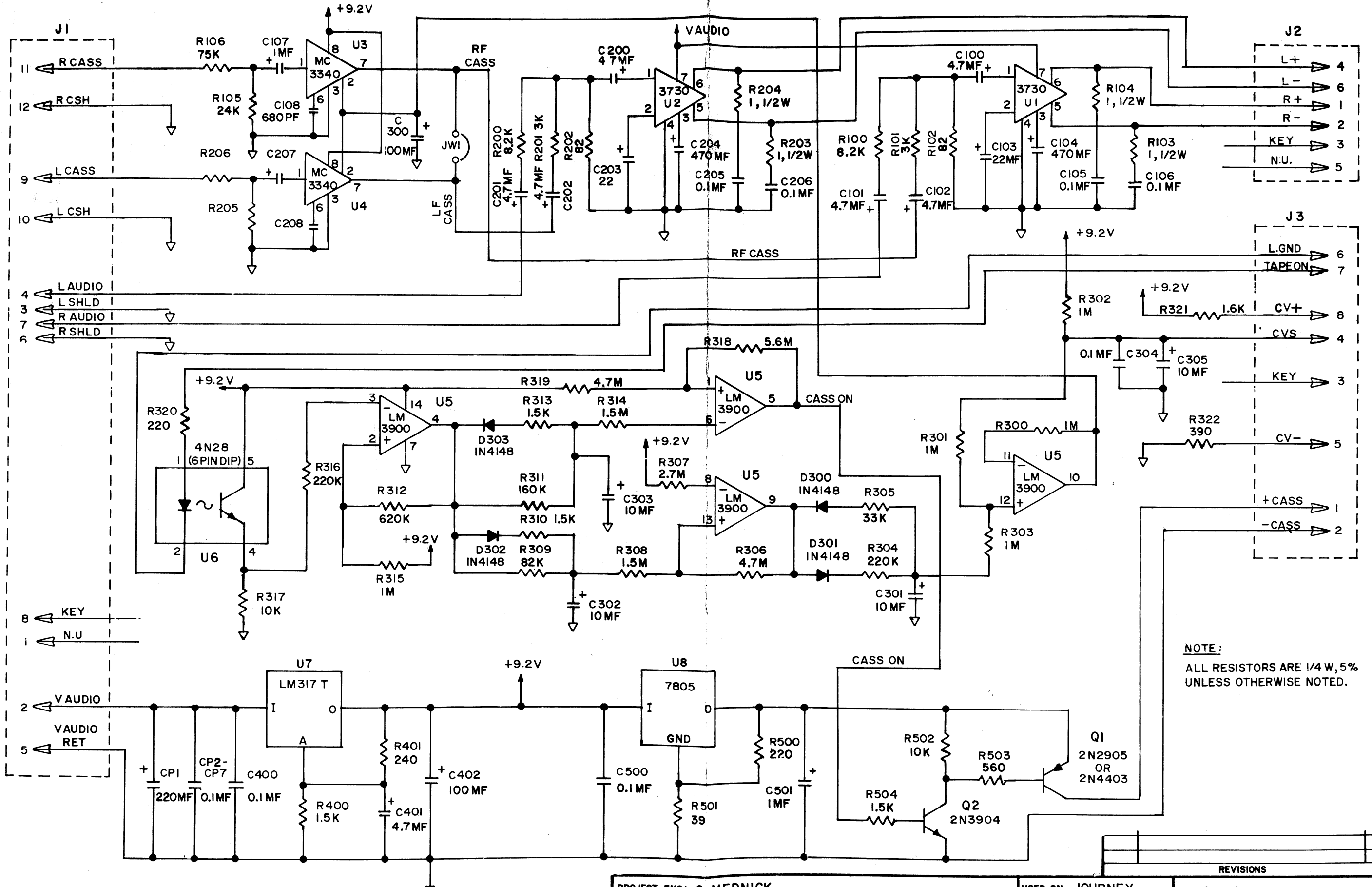
REV. (A)	INCREASED FUSE VALUES WAS 3 AMP - NOW 4 AMP ADDED PART NO. (U.L.)	MB 3-15-83
REV. (B)	INCREASED FUSE VALUE WAS 3 AMP - NOW 4 AMP	MB 3-24-83

MT 89 DOMESTIC  
MT 90 EXPORT



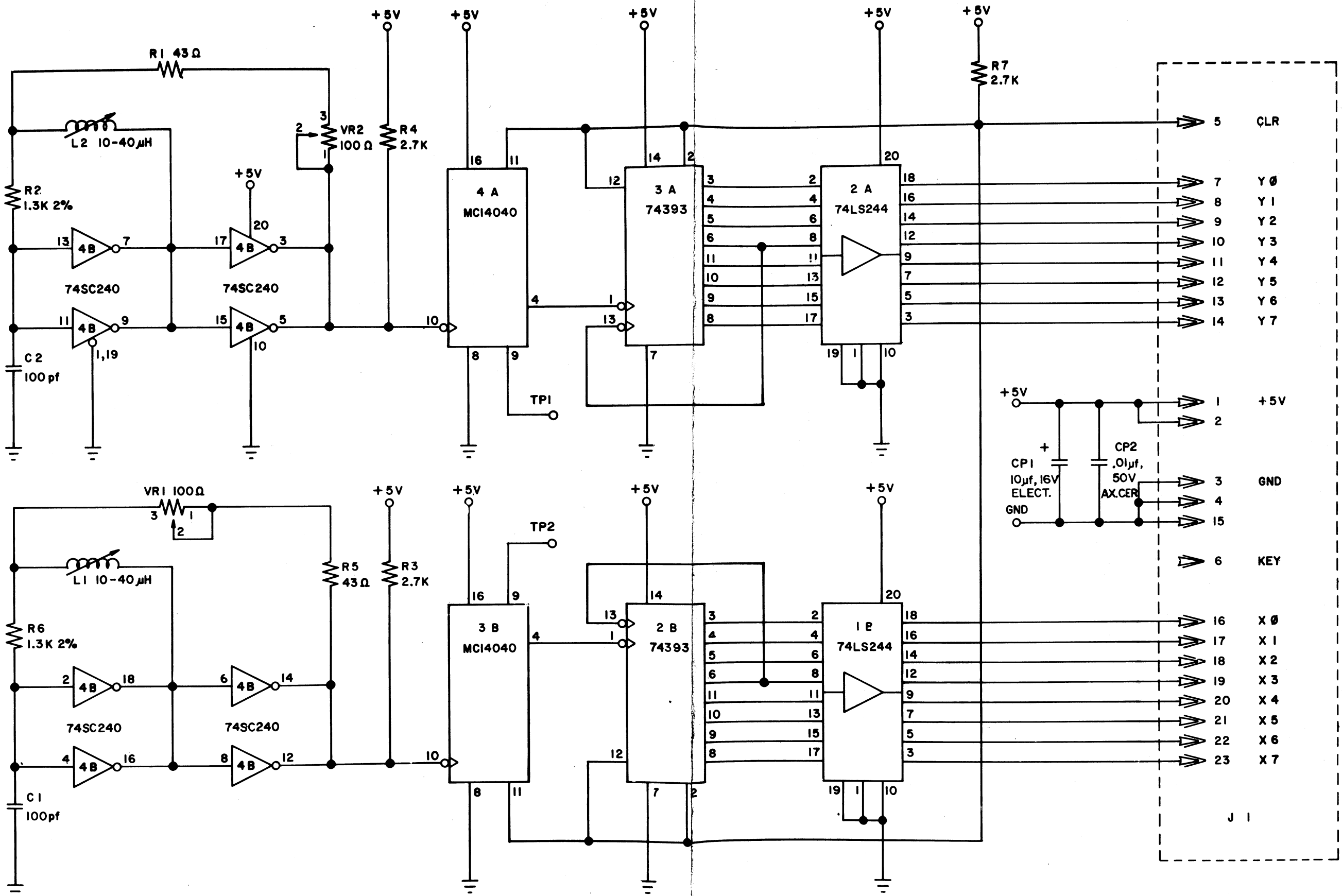
MCR-42

PROJECT ENG: L. DEKKER		DATE: 5/3/82		USED BY: SATANPROLOW		MIDWAY MFG. CO.	
DO NOT SCALE DWG.		FULL		NO REG. 1 PER.		FRANKLIN PK. ILL.	
DIM. TOLERANCES UNLESS SPECIFIED		MATERIAL		PART NO.		PART NO.	
5/3/82		POWER SUPPLY 125VA W/CKT SUPPORT A082-90412-0000		M051-00945-D007			



**NOTE:**  
ALL RESISTORS ARE 1/4 W, 5%  
UNLESS OTHERWISE NOTED.

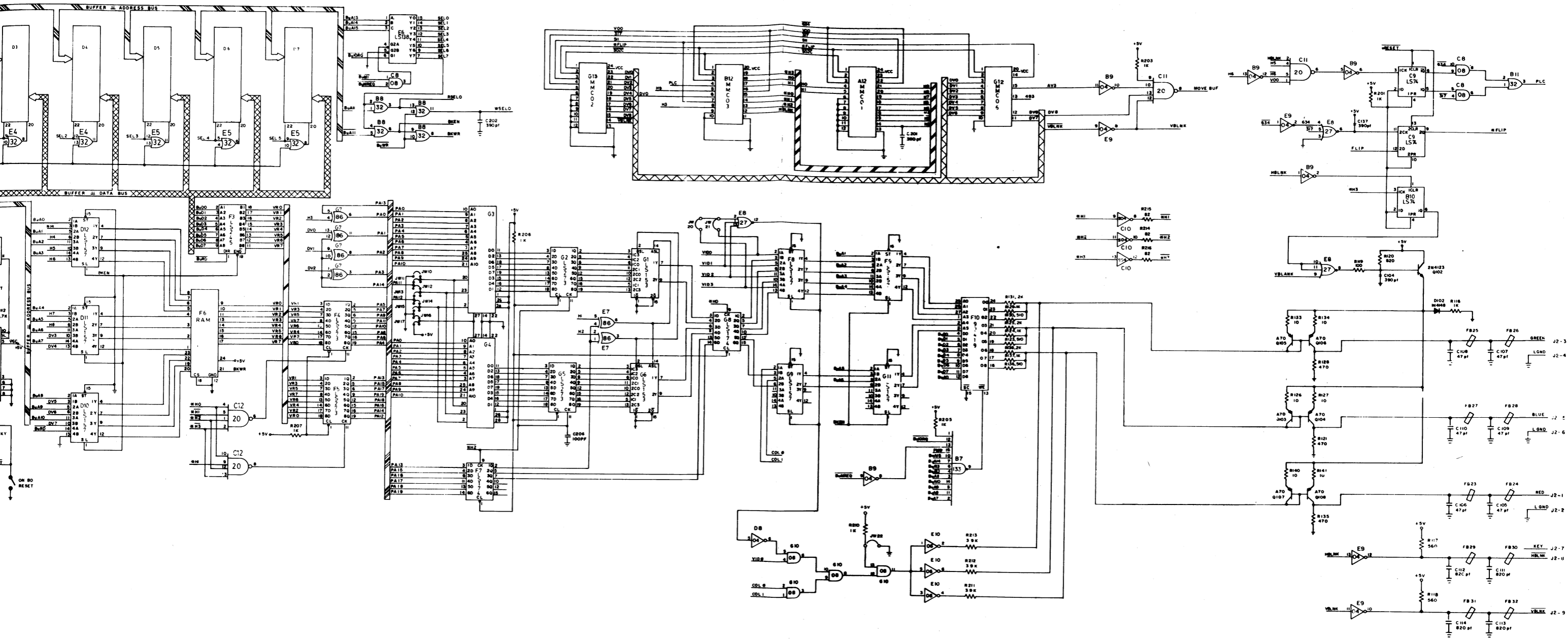
PROJECT ENG: C. MEDNICK		USED ON JOURNEY		REVISIONS	
DO NOT SCALE DWG.		HEAT TREAT	SCALE	FULL	
DIM. TOLERANCES UNLESS SPECIFIED		DRR. 138	MAP'L.	NO. REQ'D 1 PER	
CONCENTRICITY ± 0.03		CND.	FINISH	DUAL PWR AMP W/CASS INTERFACE	
FRACTIONAL 1/64		DATE 04/07'83		SCHEMATIC DWG	
DECIMAL 0.05				A084-91496- B358	
HOLE DIA +0.02 .000				PART NO.	
				M051 - 00358 - B009	
				Bally / MIDWAY MFG. CO.	
				FRANKLIN PK. ILL.	



PROJECT ENG: JOHN BOYDSTON		USED ON KOZMIKKROOZ'R		Bally / MIDWAY MFG. CO. FRANKLIN PK. ILL.	
DO NOT SCALE DWG.		HEAT TREAT	SCALE FULL	NO. REQ'D 1 PER	
DIM. TOLERANCES UNLESS SPECIFIED		DRG. G.C.	SCHEMATIC DWG, ANALOG JOYSTIC P.C.		PART NO.
CONCENTRICITY TYP 0.03		CRD. JBB	A082-91458-E000		M051-00986-E024
FRACTIONAL 1/64		DATE 2/17/83	A084-91458-E000		
DECIMAL 0.005					
MOLE DIA. +.002-.000					







DESIGNED BY: R.A. PLOUSSARD		CHECKED BY: JOURNEY		DATE: 04/15/83	
REVISED BY: (blank)		REVISED BY: (blank)		DATE: (blank)	
PART NO: M051-00304-0008		SUPER CPU MCR III		SCHEMATIC DWG	
M051-00304-0008		A082-91475-0000		PART NO: M051-00304-0008	