APPENDIX D:

EDO/FPM TIMING MEASUREMENTS

The most important parameter of a memory chip is its speed capability, which is characterized by its Access Time. The Access Time is the dominant factor in the cost of memory chips and modules. It is also the only parameter which is marked on the chips.

The primary function of a memory chip is to retrieve and to store data. Ideally, it would be very desirable if a memory chip could deliver its stored data at the exact instant of time when it receives the read command. In practice, this process does take some length of time which is generally called Access Time. Intuitively, the Access Time of a memory chip is the length of time from the moment the chip is instructed to read specific data until the point in time when the required data is available at the chip's output.

DRAM chips utilize a clever accessing scheme which allows them to address 16,000,000 cells (which require 24 address bits) by scanning the address bits in two portions (ROW and COLUMN). As a result, a 16M chip can use only 12 pins for the address bits. To load the address, two control signals, RAS (Row Address Scan) and CAS (Column Address Scan), are applied sequentially to the chip. The period of time between the initiation of the RAS signal until the instant when the data is available at the chip's output is called the DRAM Access Time. The Access Time determines the speed of a memory chip: A chip with a shorter Access Time is faster.

The chip manufacturer marks (and rates) chips with the WORST CASE condition. In other words, the manufacturer fully guarantees that the chip Access Time will either meet or exceed its marked rating under full recommended operating conditions. The industry standard "recommended operating conditions" means operating voltages from 4.5V to 5.5V, temperature from 0^{o}C to 70^{o}C, maximum capacitance load on the data-line of 100pF, and maximum data-line load of 2 TTL input loads.

SIMCHECK II measures the ACTUAL Access Time of the chip as it is subjected to the maximum recommended loading condition and under the lowest voltage within the chip specifications.

You will be surprised to see that in most cases the ACTUAL Access

Time is much better than the manufacturer's rating because most manufacturers tend to have a substantial margin of safety. However, as the DRAM technology matures (namely, chips with faster ratings), the difference between the manufacturer's rating and the ACTUAL Access Time becomes smaller: a typical 150nS rated chip may have 100nS ACTUAL Access Time at room temperature, while an 80nS rated chip may have 70nS ACTUAL Access Time at room temperature.

While SIMCHECK II helps you to sort out faster memory modules in comparison to their marked WORST-CASE Access Time, care should be taken along the following general guidelines:

1. Memory chips become slower at higher temperatures - the same chip which can run at 54nS at 25^{O}C may slow down to 68nS at 70^{O}C. Therefore, the BASIC SIMCHECK II test which is conducted at room temperature may show a better Access Time than the later EXTENSIVE test that includes the Chip-Heat mode, where the module will actually be warmed to true working temperatures.

2. Memory chips become slower at lower voltages - the same chip which can run at 90nS at 5.5V may slow down to 100nS at 4.5V. Therefore, SIMCHECK II's Access Time tests are conducted at 4.5V for 5.0V devices and at 3.0V for 3.3V devices.

3. Other speed related factors (e.g. loading conditions) may be different in your particular application as compared to the testing conditions.

After obtaining the speed of the memory module from your SIMCHECK II, determine your own margin of speed-variation and base it on the above arguments and your particular application. Experiment with modules of different actual Access Times to determine your margin of safety. We would like to emphasize that SIMCHECK II provides you with the ACTUAL Access Time reading, with no added artificial margin.

With SIMCHECK II, the actual Access Time is automatically calculated and displayed. There is no need to set an Access Time switch. The module's Access Time is determined by the slowest chip on the module and our SINGLE BIT test will also show you the speed of each chip on the module! Additionally, the Chip-Heat mode warms the module to actual working temperatures, an

important parameter in Access Time measurement.

Cycle Time Measurement

One of the unique achievements of SIMCHECK II is the ability to test the cycle time of the memory device. It is important to understand the difference between a module's cycle time and its access time. The access time of a memory device is the minimum time delay between the initiation of the access operation and the time when the accessed data is available at the device output port. The access time is the timing parameter marked on the memory chip and is readily tested by SIMCHECK II. The cycle time of the memory device is the minimum time delay from one memory access to the next. Therefore, the shorter the cycle time, the more data accesses can be performed each second (higher data rate). After each access, the DRAM device needs a time-out period (called a precharge time). This precharge time significantly slows down the cycle time of DRAM devices compared to SRAM devices, and therefore becomes a speed limiting factor in DRAM operation. SIMCHECK II's ability to test cycle time is an important feature not previously available on comparable testers. This enhances the usefulness of SIMCHECK II in determining the quality and actual operational speed of the tested memory devices.

APPENDIX E:

MODULE REPAIR WITH SIMCHECK II

SIMCHECK II is not merely a Pass/Fail tester. It is designed to provide you with explicit error data to enable you to identify the defective component/s on the DUT.

The SIMCHECK II test starts first by checking the external wiring of the DUT, then it quickly determines the structure and speed of the DUT and identifies internal wiring problems, DRAM modes (e.g. EDO), and any defective DRAM interface circuitry. After this set of quick tests, the entire memory array is thoroughly examined.

You will find the following features to be useful in your repair efforts:

1. *The Test Log:* All the test results, structure/speed information and detected errors are reported on the screen and immediately stored in the Test Log. The Test Log is accessed from STANDBY mode by pressing F4 and it contains all the information from the last test. Upon exiting the Test Log, all error menus are re-created, allowing you to extract any information you may have missed during the actual test. Even if the test is prematurely terminated once an error is detected, you can still find valuable information in the Test Log.

2. *Continuation After Error:* SIMCHECK II does not stop when it encounter errors, unless the error is FATAL in nature (like "RAS0 stuck at 0" which will terminate the test as you cannot access the DUT). You can continue to test after most error messages by pressing F1. This gives you more information as can be shown in the following example. Suppose SIMCHECK II first halts the test with an address error. If you continue the test, a bit data error may further indicate which chip/s caused the error (unless, of course, the address error is due to a connector problem common to all the chips).

3. *Advanced Setup:* You may also use the advanced setup features outlined in Section 6 to further analyze the errors. Such setup features allow you, for example, to test only part of the DUT (setup size), or you can fix the speed at much slower values. You can also check the device at specific values for Trcd, Trah,

and other parameters.

4. *SINGLE BIT Test:* SIMCHECK II's SINGLE BIT test has been significantly upgraded from our previous models, and it is now designed to give you much more information while concentrating explicitly on each bit. You can also access the SINGLE BIT test directly from STANDBY mode, enabling some investigation of those devices with fatal errors. This test is not used on SDRAM testing.

SIMCHECK II's errors generally identify the relevant pins (circuit connections to the test socket) of the DUT which are associated with the problem. You can remove the DUT from the socket and review the Test Log, which is kept in SIMCHECK II's own memory, until you start another test.

Only a technician with component-level repair expertise can repair a memory module. The required soldering/desoldering equipment is relatively complex, especially with modules and cards made with extremely thin Surface Mount technology (TSOP). Nevertheless, a few minor problems which are identified by SIMCHECK II can be repaired with simple tools. A short between an adjacent pin may be caused by a small piece of metallic debris which is stuck between two chips. You "repair" the module in this case with an Exacto knife or a watchmaker's fine screwdriver by simply removing the debris.

If you use SIMCHECK II in the production shop, you should be able to easily replace the DUT's components. You will need to convert SIMCHECK II's error notifications from pin numbers to the actual parts on your DUT.

When working with 72-pin SIMM modules or 168-pin DIMMs, you will need to have a wiring diagram of the module to identify the chip which is connected to the data line (DQ pin) which was identified as bad by SIMCHECK II. We have included some tables of JEDEC pin numbers in Appendix E. Module wiring diagrams and DRAM chip data sheets are available from their manufacturers.

If you do not have the actual wiring for the DUT, do not despair. With hundreds of DUT board designs available, wiring diagrams are hard to find. You can, however, use a continuity meter from the pin identified by SIMCHECK II to find the connected chip. Please note that with data (DQ) type error, you can identify the actual defective chip, taking care to work on the DUT's BANK (B1, B2, etc.)

identified by SIMCHECK II. If the problem is with address lines that are common to all chips, you may need to run more tests (press F1 to Continue when the address error is first reported) or use the SINGLE BIT test to find a relation between the address line problem and a particular chip. Of course, if the address line problem is on the trace to the DUT's connector, the address error is common to all chips.

If you work with the older 30 pin SIMMs, identification is typically easier. For example, if the module is made up of 8 or 9 chips, bit 1 is in the chip closest to pin 1 of the module. Bit 2 is the second chip and so forth. If the module is made with three chips, then bits 1 to 4 are in the left chip (the one closest to pin 1), and bits 5 to 8 are in the middle chip. Bit 9 is in the furthest right chip.

APPENDIX F:

MEMORY MODULE TECHNICAL REVIEW

Throughout the computer era, the need for faster and denser memory devices has put constant pressure on memory manufacturers. The push to maximize memory capabilities has resulted in ever-changing technology.

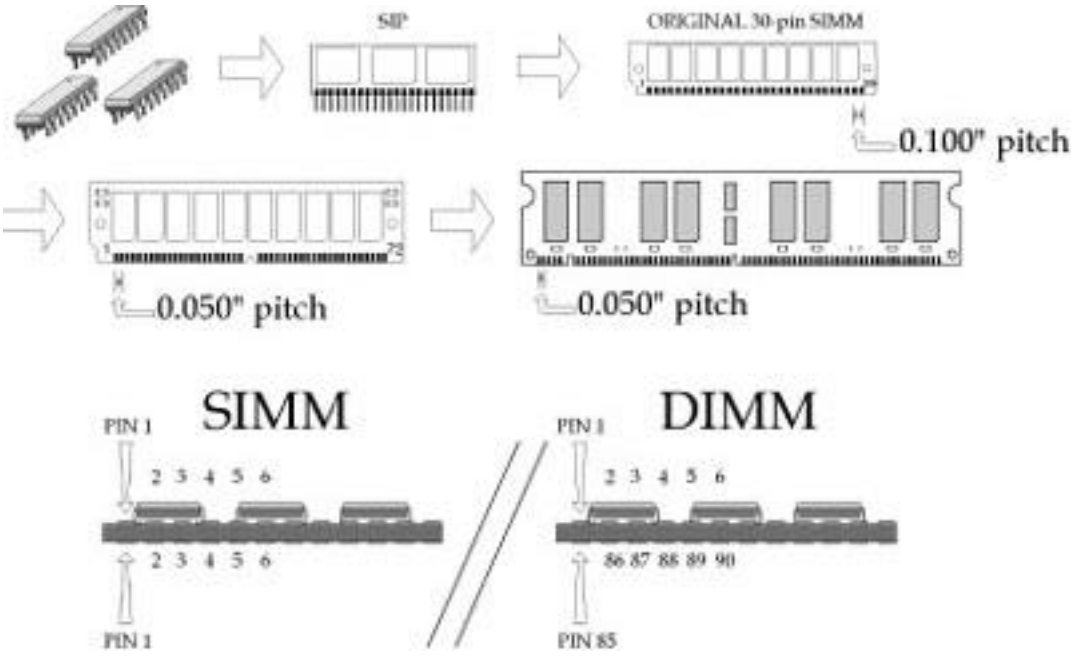
The Evolution of the DIMM Module

In the early and mid-80s, memory modules were made in a variety of pinouts and without any dominant standards. Early PCs used individual DRAM chips on the motherboard. An early module, the TM4164EQ5 had five such chips on a 24-pin module to achieve a 64Kx5 module.

The first 22-pin SIP (Single Inline Package) modules appeared in the early 80s, comprised of memory devices mounted on a PCB with 22 interconnection pins spaced at 0.100" intervals along a line. Memory modules became popular only after the Wang Laboratories invention of the SIMM (Single Inline Memory Module) technology, where the SIP's legs have been replaced by an edge connector and a convenient mounting feature which includes a special tab to identify pin 1 and two mounting holes.

By the early 90s, most computer systems switched to the SIMM technology due to greater space saving capabilities. Original SIMMs had 30 contacts (pins) which were spaced apart at 0.100". Although contacts for the SIMM device appear on both sides of the edge connector, all opposite contacts are shorted together across the board to achieve more reliable contact with the SIMM socket (see illustration). With the 30-pin limited to 16Mx9, IBM extended the SIMM pin count to 72 for their PS/2 computers, thus allowing for modules with 16Mx36 or x40 bits. To make the PS/2 SIMM module small, the spacing between the contacts was halved to 0.050", but opposite contacts were still shorted across the edge connector.

All solid state memory configurations are now coordinated and standardized by the Electronic Industries Association through its JEDEC Standard 21-C.



The emergence of 64-bit Pentiums triggered the need for modules with a data bus supporting at least 64 bits. The 72-pin SIMM did not have enough pins to accommodate such a wide bus since many additional pins are required for the address, control and power connections. As a result, the DIMM (Dual Inline Memory Module) originated. Improvements in socket technology assured reliable contacts on both sides of the edge connector. The advent of DIMMs made use of these contacts, in effect doubling the connection density of the SIMM.

The first DIMM devices were the 72-pin DIMMs and the 168-pin DIMMs. The 72-pin DIMM is intended for mere size reduction of a 72-pin SIMM for use in portable computers. The 168-pin DIMMs allow for 64-80 bits configuration, and are used for both Standard DRAM and Synchronous DRAM (SDRAM) modules. Recently added is the 144-pin DIMM, with more configurations to be expected.

The following is the JEDEC standard pin-out of the 30-pin modules:

PIN	ITEM	DESCRIPTION
1	+Vcc	+5V
2	-CAS	Column Address Strobe
3	DQ1	Data I/O bit 1

4	A0	Multiplexed Address bit 0
5	A1	Multiplexed Address bit 1
6	DQ2	DATA I/O bit 2
7	A2	Multiplexed Address bit 2
8	A3	Multiplexed Address bit 3
9	GND	Ground
10	DQ3	DATA I/O bit 3
11	A4	Multiplexed Address bit 4
12	A5	Multiplexed Address bit 5
13	DQ4	DATA I/O bit 4
14	A6	Multiplexed Address bit 6
15	A7	Multiplexed Address bit 7
16	DQ5	DATA I/O bit 5
17	A8	Multiplexed Address bit 8
18	A9	Multiplexed Address bit 9
19	A10	Multiplexed Address bit 10
20	DQ6	DATA I/O bit 6
21	-W	Write Command
22	GND	Ground
23	DQ7	DATA I/O bit 7
24	A11	Multiplexed Address bit 11
25	DQ8	DATA I/O bit 8
26	Q9	DATA OUT bit 9
27	-RAS	Row Address Strobe
28	-CAS9	BIT 9 Column Address Strobe
29	D9	DATA IN bit 9
30	+Vcc	+5V

Notes:

- In an eight-bit configuration, pins 26, 28, and 29 are NC (not connected).
- A8 to A11 are NC in 64K modules.
- A9 to A11 are NC in 256K modules.
- A10 to A11 are NC in 1M modules.
- A11 is NC in 4M modules.
- "-" in front of a signal name like "-RAS" indicates a control line which is "Active Low". (A bar over the signal name is another industry convention.)

The JEDEC standard pin-out of the 72-pin module is detailed in the following table:

PIN	x36	x40	DESCRIPTION
1	GND	GND	Ground
2	DQ0	DQ0	Data I/O

3	DQ18	DQ1	Data I/O
4	DQ1	DQ2	Data I/O
5	DQ19	DQ3	Data I/O
6	DQ2	DQ4	Data I/O
7	DQ20	DQ5	Data I/O
8	DQ3	DQ6	Data I/O
9	DQ21	DQ7	Data I/O
10	+Vcc	+Vcc	+5V
11	NC	NC	No Connection
12	A0	A0	Multiplexed Address bit 0
13	A1	A1	Multiplexed Address bit 1
14	A2	A2	Multiplexed Address bit 2
15	A3	A3	Multiplexed Address bit 3
16	A4	A4	Multiplexed Address bit 4
17	A5	A5	Multiplexed Address bit 5
18	A6	A6	Multiplexed Address bit 6
19	A10	-OE	x36: Multiplexed Address bit 10 x40: Output Enable
20	DQ4	DQ8	Data I/O
21	DQ22	DQ9	Data I/O
22	DQ5	DQ10	Data I/O
23	DQ23	DQ11	Data I/O
24	DQ6	DQ12	Data I/O
25	DQ24	DQ13	Data I/O
26	DQ7	DQ14	Data I/O
27	DQ25	DQ15	Data I/O
28	A7	A7	Multiplexed Address bit 7
29	NC	DQ16	x36: No Connection x40: Data I/O
30	+Vcc	+Vcc	+5V
31	A8	A8	Multiplexed Address bit 8
32	A9	A9	Multiplexed Address bit 9
33	-RAS3	NC	x36: Row Address Strobe 3 x40: No Connection
34	-RAS2	NC	x36: Row Address Strobe 2 x40: No Connection
35	DQ26	DQ17	Data I/O
36	DQ8	DQ18	Data I/O
37	DQ17	DQ19	Data I/O
38	DQ35	DQ20	Data I/O
39	GND	GND	Ground
40	-CAS0	-CAS0	Column Address Strobe 0
41	-CAS2	A10	x36: Column Address Strobe 2 x40: Multiplexed Address bit 10
42	-CAS3	A11	x36: Column Address Strobe 3 x40: Multiplexed Address bit 11
43	-CAS1	-CAS1	Column Address Strobe 1
44	-RAS0	-RAS0	Row Address Strobe 0
45	-RAS1	-RAS1	Row Address Strobe 1
46	NC	DQ21	x36: No Connection x40: Data I/O
47	-W	-W	Write Command
48	NC	GND	x36: No Connection x40: Ground
49	DQ9	DQ22	Data I/O
50	DQ27	DQ23	Data I/O
51	DQ10	DQ24	Data I/O
52	DQ28	DQ25	Data I/O
53	DQ11	DQ26	Data I/O

54	DQ29	DQ27	Data I/O
55	DQ12	DQ28	Data I/O
56	DQ30	DQ29	Data I/O
57	DQ13	DQ30	Data I/O
58	DQ31	DQ31	Data I/O
59	+Vcc	+Vcc	+5V
60	DQ32	DQ32	Data I/O
61	DQ14	DQ33	Data I/O
62	DQ33	DQ34	Data I/O
63	DQ15	DQ35	Data I/O
64	DQ34	DQ36	Data I/O
65	DQ16	DQ37	Data I/O
66	NC	DQ38	x36: No Connection x40: Data I/O
67	PRD1	PRD1	Presence Detect 1
68	PRD2	PRD2	Presence Detect 2
69	PRD3	PRD3	Presence Detect 3
70	PRD4	PRD4	Presence Detect 4
71	NC	DQ39	x36: No Connection x40: Data I/O
72	GND	GND	Ground

Memory chips are internally arranged in a ROW/COLUMN matrix selection (actual architectures are somewhat more complex but conceptually the same). -RAS is used to strobe the ROW address lines and -CAS is used to strobe the COLUMN address. As a result, only 11 address lines are needed to create the real address of 22 bits required for 4Meg modules. DRAM memory chips operate in accordance with a variety of protocols (namely, the order of –RAS, -W, and -CAS and other control signals). Interested readers should refer to memory data sheets for more details. SIMCHECK II has full software control of all the module pins and it can test the behavior of the module under most possible protocols.

True 3.3V Testing

The overall trend toward 3.3V was initially inspired by the goal of reducing power. In complex devices like CPUs and DRAMs, the shrinking geometry of the manufacturing process creates an unwanted large electrical field between silicon regions of opposite charges which may break the thin dielectric isolation layers. Reducing the main voltage from 3.3V shrinks these electrical fields thus allowing for smaller geometry and higher DRAM densities. SIMCHECK II includes special circuitry to perform true 3.3V testing, which means that all signals to the DUT (device under test) are set within the 3.3V range, not just the power supply. Voltage tests change the voltages to the range of 3.0V-3.6V.
In addition to 3.3V and 5V testing, the actual test voltage may be set up to other levels by the user.

APPENDIX G:

SIMCHECK II EXPANSION PORT

SIMCHECK II's design allows ample room for expansion and enhancement using its 40-Bit Expansion Port (behind the 72-pin SIMM socket) and its 96-pin DIN side socket. In addition to standard adapters, we design customized adapters for customer's proprietary modules. Alternatively, we can also support customers in their in-house development of their own special adapters.

This appendix presents some introductory information on SIMCHECK II's expansion. Please contact us for more detailed examination of your specific requirements.

The SIMCHECK II's Expansion Ports as well as its entire design is a protected intellectual property of INNOVENTIONS Inc. Information given in this section is intended for customers building their own in-house adapters to use in conjunction with SIMCHECK II.

The most effective way to design a customized adapter for testing non- standard memory devices is to connect the adapter directly to the 40-Bit Expansion Port. This socket has 40 data lines (DQ type), 16 address lines, 4 RAS lines, 4 CAS lines, two write lines, four PRD lines, numerous power lines, and several special purpose lines.

Our DIMMCHECK 168P option adapter (p/n INN-8484-9) is a good example illustrating how we have used this port to test DIMMs with up to 80 data lines, 8 CAS lines, 2 Id lines and 8 PRD lines.

Our CUSTOMIZED ADAPTER (p/n INN-8484-1) can serve as a basic breadboard for the development of your own adapters.

The SIMCHECK II 40-Bit Expansion Port is a 45x2 DIN connector. The following is the pin list of this proprietary bus expansion slot.
Pin numbering: The bottom-left pin is pin 1. Pin 2 is the top-left pin. Numbering continues in a zigzag fashion across the connector. Pin 89 is the bottom-right pin, and pin 90 is the top-right pin.

Pin #	Function	Pin #	Function	Pin #	Function
1	+5V	31	DQ22	61	DQ9
2	-W1	32	DQ7	62	DQ28
3	SEL1	33	DQ23	63	DQ10
4	VDD2	34	MA7	64	DQ29
5	MA12	35	MA11/DQ16	65	DQ11
6	MA13	36	VDD main	66	DQ30
7	GND	37	MA8	67	DQ12
8	DQ0	38	MA9	68	DQ31
9	DQ16	39	-RAS3	69	VDD main
10	DQ1	40	-RAS2	70	DQ32
11	DQ17	41	MDQ26	71	DQ13
12	DQ2	42	MDQ8	72	DQ33
13	DQ18	43	GND	73	DQ14
14	DQ3	44	VDD main	74	DQ34
15	DQ19	45	GND	75	DQ15
16	VDD main	46	VDD main	76	MDQ38
17	-CASP	47	MDQ17	77	PRD1
18	MA0	48	MDQ35	78	PRD2
19	MA1	49	GND	79	PRD3
20	MA2	50	-CAS0	80	PRD4
21	MA3	51	-CAS2/A10	81	MDQ39
22	MA4	52	-CAS3/A11	82	GND
23	MA5	53	-CAS1	83	SEL2
24	MA6	54	-RAS0	84	MA10
25	MA10/OE	55	-RAS1	85	MA15
26	DQ4	56	MDQ21	86	MA11
27	DQ20	57	-W0	87	MA14
28	DQ5	58	ECC	88	SEL3
29	DQ21	59	DQ8	89	SEL4
30	DQ6	60	DQ27	90	+5V

NOTES:

- This port is upward compatible with the SIMCHECK 40-BIT PORT. Not all the signals are the same.
- MDQ lines are multiplexed with additional functions.
- Do not connect VDD2 (pin 4) to any of the other VDD main lines.
- SEL1-4 are software controlled and may not be used in customized adapters that will not require program modification.
- Some lines (e.g. MA10, 11) are duplicated on purpose to avoid shared lines.

APPENDIX H:

SIMCHECK II MAINTENANCE

Please calibrate periodically. Factory calibration at regular intervals keeps your unit current to existing specifications.

H.1 CALIBRATION & UPGRADE

Although system calibration is not an absolute requirement for SIMCHECK II/IIse PLUS, we do strongly recommend that you have your unit serviced periodically. This makes sure that it remains current to factory production specifications and operates at its most optimum level, thereby protecting your investment and ensuring that your test system does not become obsolete.

We recommend that each unit undergo a factory calibration & upgrade every 12-18 months. Additional information regarding what the upgrade covers can be obtained by visiting our website.

H.2 SIMCHECK II INTERNAL ARCHITECTURE

Referring to Figure 1, SIMCHECK II is made up of two PCBs joined together through a 96-pin connector. SIMCHECK II can be opened by removing the six anti-skid rubber feet, then removing the six corresponding phillips screws from the bottom of the enclosure. Once these screws are removed, you can simply lift up the top shell, as shown in Figure 1. The SIMCHECK II keyboard and the 128x32-pixel LCD board are attached to the lower PCB (also known as the Processor Board) using solderless connectors and screws. The top board, known as the SIMM Board, can be detached at the 96-pin connector.

H.3 Replacement of 30 or 72 pin sockets

The sockets used by SIMCHECK II are attached to the internal PCB with the use of solderless pin receptacles, or barrel sockets. Therefore, socket replacement is almost effortless, as no desoldering is required.

Socket Removal

1. Referring to Figure 1, remove the (6) anti-skid rubber feet, then the screws (#4x3/8 machine phillips).

2. Separate the case halves to expose the circuit boards.

3. Remove the (6) retaining screws (4/40 x 5/16 phillips) from the top circuit board. Pull top circuit board straight up, separating it from the bottom board as shown in Figure 2**.**

4. Remove the (2) screws (4/40 x 7/16 Black Oxide Pan Head) and black fiber washers**.**

5. Gently, using a rocking motion, pull to separate the socket from the circuit board.

Socket Insertion

1. Assure that there is no debris in the area where the new socket is to be placed.

2. Align the pins of the socket with the barrel sockets and gently push using a slight rocking motion.

3. Replace (2) screws (4/40 x 7/16 Black Oxide Pan Head) and fiber washers and tighten (Avoid damaging the circuit board by over tightening). See Figure 2**.**

4. Replace the top circuit board and replace (6) screws (4/40 x 5/16 Phillips) and washers (do not over tighten)**.**

5. Place the case halves back together and replace (6) screws (#4 x 3/8 machine Phillips), do not over tighten. Replace the rubber feet**.**

Refer to Section 4.3 for additional information on adjusting the LCD.

H.4 CHANGING JUMPER SETTINGS

Figure 4 illustrates the jumpers on the SIMCHECK II's processor board. These jumpers are setup at the factory and you will rarely need to modify them. You will not need to change JP1 and P7 as they are used for board testing only.
JP6 controls the intensity of the LCD backlighting. It is set by default for LOW backlight, however, if you wish to switch to HIGH backlight, you may set JP6 to the upper most settings.

JP5 controls the size of the SRAM chips installed in your board, which is currently 64KB SRAM. There may come a point when SIMCHECK II's SRAM chips will be upgraded to 128KB or 256KB, which requires setting the JP5 jumper to the left.

FIGURE 1
SIMCHECK II INTERNAL ARCHITECTURE

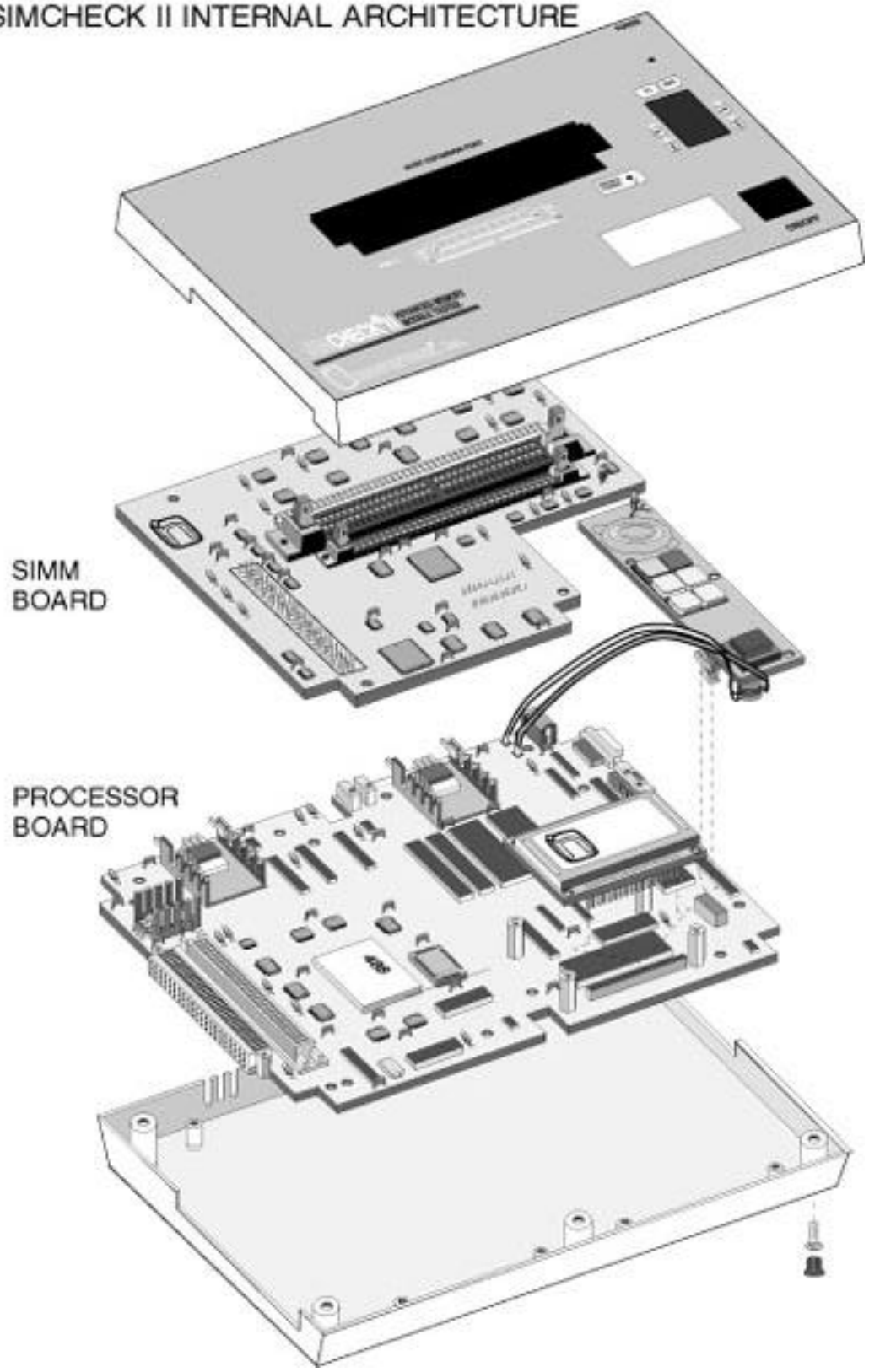


FIGURE 2

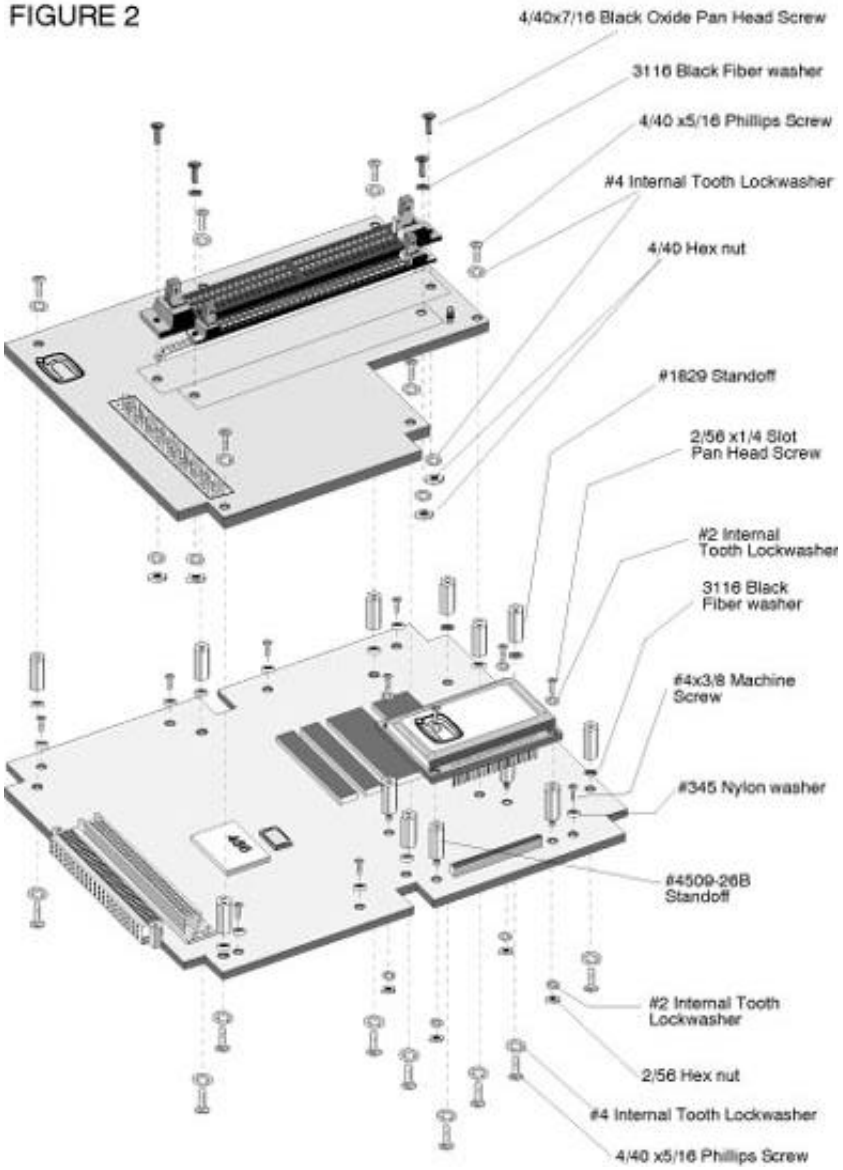

4/40x7/16 Black Oxide Pan Head Screw
3116 Black Fiber washer
4/40 x5/16 Phillips Screw
#4 Internal Tooth Lockwasher
4/40 Hex nut
#1829 Standoff
2/56 x1/4 Slot Pan Head Screw
#2 Internal Tooth Lockwasher
3116 Black Fiber washer
#4x3/8 Machine Screw
#345 Nylon washer
#4509-26B Standoff
#2 Internal Tooth Lockwasher
2/56 Hex nut
#4 Internal Tooth Lockwasher
4/40 x5/16 Phillips Screw

FIGURE 3

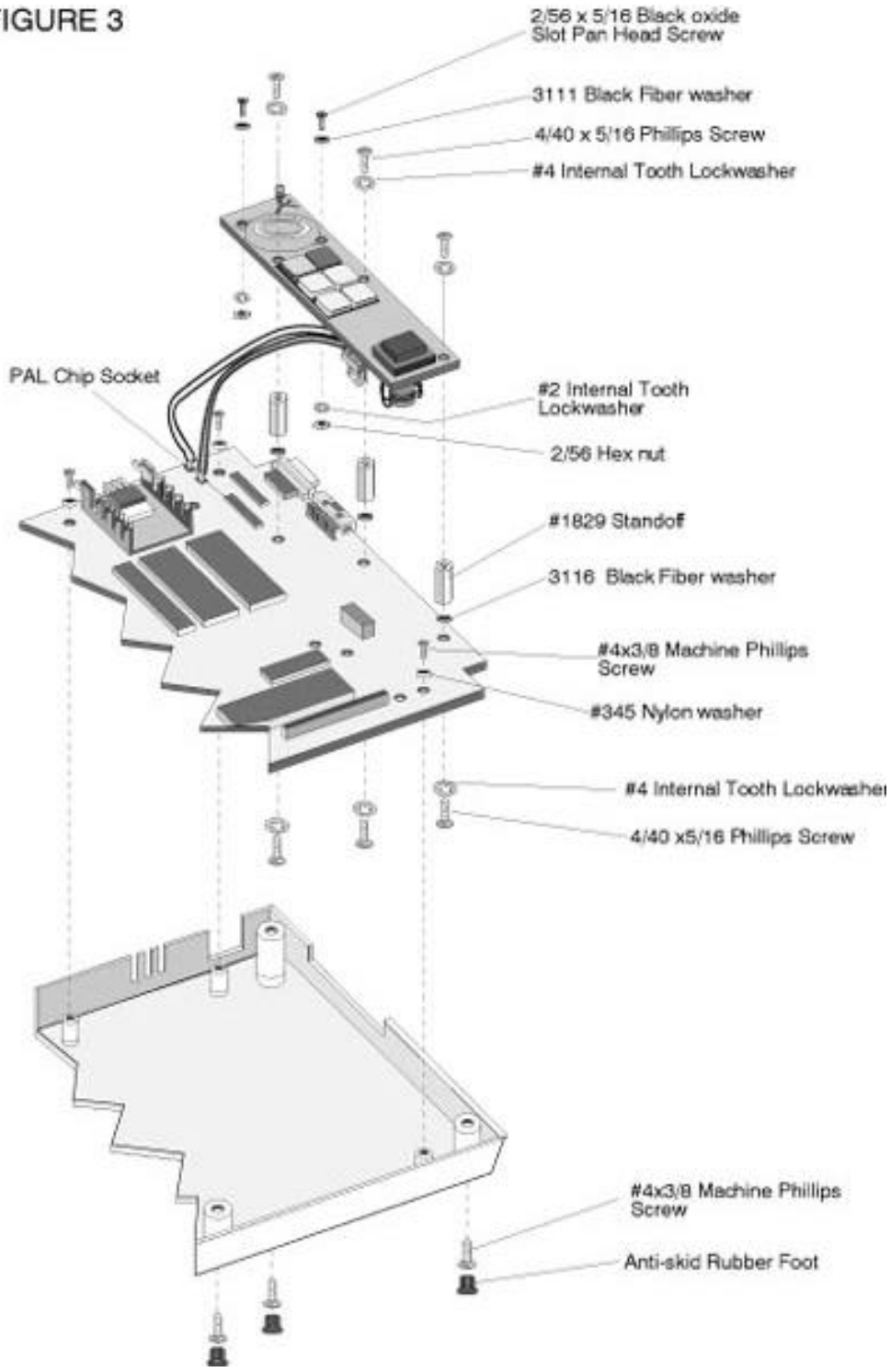
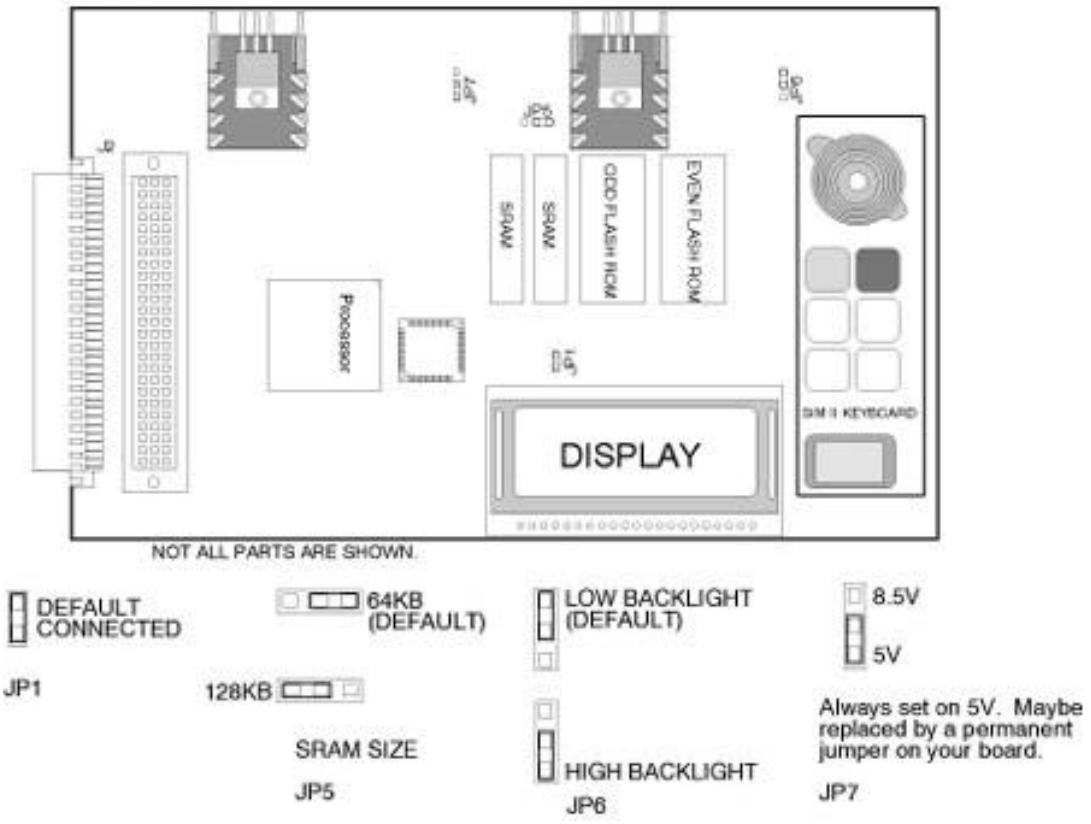

2/56 x 5/16 Black oxide
Slot Pan Head Screw
3111 Black Fiber washer
4/40 x 5/16 Phillips Screw
#4 Internal Tooth Lockwasher
PAL Chip Socket
#2 Internal Tooth
Lockwasher
2/56 Hex nut
#1829 Standoff
3116 Black Fiber washer
#4x3/8 Machine Phillips
Screw
#345 Nylon washer
#4 Internal Tooth Lockwasher
4/40 x5/16 Phillips Screw
#4x3/8 Machine Phillips
Screw
Anti-skid Rubber Foot

FIGURE 4



H.5 HANDLER/PRINTER PAL CHIP

SIMCHECK II comes with a 16-pin IDC connector to support the optional Automatic Device Handlers and the Direct Printer Interface. This IDC connector is controlled by the special PAL chip that comes with your Handler or Direct Printer Interface options. The Handler PAL chip also supports the Direct Printer Interface, but the one supplied with the Direct Printer Interface needs to be replaced if you plan to use the Handler. This section explains how to install this PAL chip into the designated socket inside SIMCHECK II (see Figure 3).

You must first remove the six rubber feet and their corresponding phillips screws from the bottom of the SIMCHECK II enclosure (Refer to Figure 1). This will allow it to be separated and reveal SIMCHECK II's internal architecture.

The socket U18 for the PAL chip is located underneath the SIMCHECK II KEYBOARD. Remove the three 4/40 x 5/16 phillips screws from the keyboard (Figure 3) and gently disconnect

the keyboard from the Processor Board (the bottom PCB of SIMCHECK II).

Install the special PAL chip that is enclosed with your SIMCHECK HANDLER companion into the empty socket marked U18 (See Figure 3) located just below the electrolytic capacitors on the Processor Board.

Reconnect the keyboard to the Processor Board and secure it with the three phillips screws. Close the SIMCHECK unit and test your installation with your new Handler or Direct Printer Interface.

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