8

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EFFECTS OF MENU CHANGES

The 1240 does not allow illegal setup conditions to exist. As a result, changes you make in one menu may affect selections available in other menus. Tables 8-1 to 8-4 list the crucial changes and their effects.

The 1240 changes entries in other menus only when you **exit** the altered menu. If you make a change then reverse it before leaving the menu, no change is made to other menus.

Table 8-1
EFFECTS OF CHANGES TO THE OPERATION LEVEL MENU

If You Change:	EFFECTS ON OTHER MENUS ARE:
To Level 0 from higher levels	MEMORY CONFIG: Memory width vs. depth select fields are changed to fixed values that indicate no memory chaining. These values depend on the number of 9-channel and 18-channel acquisition cards installed; refer to Tables 3-1 and 3-2. TRIGGER SPEC: The LOOK FOR TRIGGER field is not displayed. The 1240 will accept a trigger only after the required amount of pre-trigger data (determined by the TRIGGER POSITION field) has been acquired.
To Levels 0 or 1 from higher levels	TIMEBASE: The ACTIVE TIMEBASES field is not displayed, and the 1240 uses only timebase T1. Timebase T2 fields are not displayed. MEMORY CONFIG: The INPUT POD and TIMEBASE fields are changed to fixed values; no selections are available. T1 is assigned to all pods. CHANNEL GROUPING: All groups are assigned T1. TRIGGER SPEC: T1 is assigned to all levels of the sequential event recognizer, and the timebase select field in each sequence level is no longer displayed. WITH STORAGE fields are not displayed in the sequential event recognizer. SEARCH PATTERN ENTRY: All lines of the pattern are set to T1, and the ENTER DATA FOR field is not displayed.
To Levels 0 or 2 from 1 or 3	TIMEBASE: GLOBAL EVENT = **CLOCKED/UNCLOCKED** field is not displayed. Events are compared to the global event recognizer only if they coincide with a sample point (CLOCKED). TRIGGER SPEC: The FILTER fields in both event recognizers are not displayed. To be recognized, an event must be present for at least one timebase period.

Table 8-2
EFFECTS OF CHANGES TO THE TIMEBASE MENU

If You Change:	EFFECTS ON OTHER MENUS ARE:
Active Timebases	MEMORY CONFIG: Each obsolete timebase assignment is changed to the legal value. For example: if you change ACTIVE TIMEBASE from **T1 AND T2** to **T2 ONLY**, all timebase assignments in Memory Config are changed to T2.
Active Timebase to T1 ONLY	MEMORY CONFIG: INPUT POD fields on the right side of the display are set to the odd-numbered pod. CHANNEL GROUPING: All groups are assigned T1. TRIGGER SPEC: T1 is assigned to all levels of the sequential event recognizer. The FILTER timebase in the global event recognizer is changed to T1. SEARCH PATTERN ENTRY: All lines of the search pattern are set to T1.
Active Timebase to T2 ONLY	MEMORY CONFIG: If T2 is SYNC, INPUT POD fields on the right side of the display are set to the odd-numbered pod. CHANNEL GROUPING: All groups are assigned T2. TRIGGER SPEC: T2 is assigned to all levels of the sequential event recognizer. All glitch entries are changed to don't care (X). The FILTER timebase in the global event recognizer is changed to T2. SEARCH PATTERN ENTRY: All lines of the search pattern are set to T2.
T1 to SYNC	TRIGGER SPEC: All glitch entries are set to don't care.
T2 to SYNC	MEMORY CONFIG: All T2 L and T2 F timebase assignments are changed to T2.
T2 to DEMUX	MEMORY CONFIG: All T2 timebase assignments are changed to T2 L.
T1 to ASYNC 10 NS when T1 and T2 are active	TIMEBASE: T1 qualifier fields are not displayed. The 1240 does not support clock qualification for T1 when T1 and T2 are active and T1 is ASYNC 10 NS.
T1 to ASYNC 10 NS when T1 ONLY is selected	TRIGGER SPEC: WITH STORAGE fields in the sequential event recognizer are not displayed.
GLOBAL EVENT field to UNCLOCKED	TRIGGER SPEC: All glitch entries in the global event recognizer are set to don't care (X).

Table 8-3
EFFECTS OF CHANGES TO THE MEMORY CONFIG MENU

If You Change:	EFFECTS ON OTHER MENUS ARE:
Memory width to a smaller number of channels	CHANNEL GROUPING: Deleted channels are removed from all groups. TRIGGER SPEC: Deleted channels are removed from both event recognizers. AUTO-RUN SPEC: If you are using the COMPARE ACQMEM TO REFMEM condition, the deleted channels are removed from the mask field. SEARCH PATTERN ENTRY: The deleted channels are removed from the search pattern.
Pod-Timebase assignments	TIMEBASE: If T1 is ASYNC with a 10 ns period and you assign T1 to any pod connected to an 18-channel card, the clock period is changed to 20 ns. CHANNEL GROUPING: If the pod-timebase change affects all channels in a group, the group is assigned the new timebase; no channels are deleted. If the change affects only some of the channels in a group, those channels are deleted from groups and appear in the UNUSED list. TRIGGER SPEC: If a pod's timebase assignment changes from an ASYNC to a SYNC timebase, all glitch entries for channels from that pod are changed to don't care (X). If the pod-timebase change affects only some of the channels in a group, those channels are deleted from both event recognizers. AUTO-RUN SPEC: If the pod-timebase change affects only some of the channels in a group, those channels are deleted from the MASK fields in COMPARE ACQMEM TO REFMEM. SEARCH PATTERN ENTRY: If the pod-timebase change affects only some of the channels in a group, those channels are deleted from all lines of the search pattern.
GLITCHES to OFF	TRIGGER SPEC: All glitch entries are set to don't care.
GLITCHES to ON	TIMEBASE: If T1 is ASYNC with a period of 10 ns, the period is changed to 20 ns.

Table 8-4
EFFECTS OF CHANGES TO THE CHANNEL GROUPING MENU

If You Change:	EFFECTS ON OTHER MENUS ARE:
Group definition by deleting or re-arranging channels	TRIGGER SPEC: Event recognizer values for the affected channels are removed or rearranged to correspond to the new group definitions. AUTO-RUN SPEC: If you are using the COMPARE ACQ-MEM TO REFMEM condition, MASK field values for the affected channels are removed or rearranged. TIMING DIAGRAM: Channels that are deleted or moved in Channel Grouping are turned **OFF** in the Timing Diagram PAGE displays. SEARCH PATTERN ENTRY: Values for the affected channels are removed from, or rearranged in, all search pattern lines.

Table 8-5
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
SAFETY		
General		Complies with the requirements of UL 1244, IEC 348, and CSA 556B.
CRT		UL, VDE (German X-radiation law).
PRIMARY POWER INPUT		
High Line		132 V or 250 V
Low Line		90 V or 180 V
Frequency		48 to 440 Hz
Power		500 VA max., 5 A max.
VIDEO OUT		Conforms to RS170
GLOBAL EVENT		Event consists of inputs from all groups.
Filter, global event UNCLOCKED		An event is not recognized unless it is accepted by the global filter. These specifications are based on a 1240 equipped with P6460 Data Acquisition Probes.
Separate 1240D1 and 1240D2 events		N is value of FILTER field; selections are 1-16. T is value of ON field (filter timebase); selections are T1 (when T1 active), T2 (when T2 active), and 10NS.
When N = 1: min. guaranteed event accepted	Timebase period + 6 ns	
When N = 2-16: max. guaranteed event rejected	(N−1) x T − 8 ns	
min. guaranteed event accepted	(N x T) + 2 ns	
Mixed 1240D1 and 1240D2 events		
max. guaranteed event rejected	(N−1) x T − 8 ns	N = 2-16
min. guaranteed event accepted	(N x T) + 20 ns	N = 1-16
Filter, global event CLOCKED		N is value of FILTER field; selections are 1-16. T is value of ON field (filter timebase) and selection (T1, T2, 10NS) is same as sample clock. Filtered event becomes valid on Nth contiguous valid acquisition event.
Accept 1240D1 &/or 1240D2 events	N x T	Combined 1240D1 and 1240D2 ASYNC acquisition requires additional 2 ns word width.
STORE ON action	clocked:	unclocked:
T1 event or T2 event	Store data if event true for 20 ns or more.	Data valid ± 12 ns - 20 ns with respect to data clock
T1 event and T2 event	Store data for a timebase if both events meet indiv. timebase spec. and the other timebase event is valid for 10 ns after storage clock.	Data valid ± 12 ns - 20 ns with respect to data clock

Table 8-5 (cont.)
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
RESET	40 ns	Counter/timer reset takes 100 ns prior to restart.
TRIGGER		Trigger position is within one stored clock of event causing trigger. If reset and trigger occur together, a trigger occurs. When AFTER MEMORY FULL is the trigger position, a trigger before memory is full causes a reset. If the counter/timer causes a trigger at the same time that the sequential event causes a reset, the 1240 will trigger and the counter/timer will be set to 0.
COUNTER/TIMER		
COUNT mode INCR CNTR	One count per valid evt.	Range is 1 to 99,999,999,999 events
TIME mode TIME WHILE	Accuracy, start to stop: ± 20 ns	Timer value truncated to 4 digits. Filter clk. must equal sample clk.
SEQUENTIAL EVENT		Event may consist only of groups assigned the same timebase.
Filter, accept event	N x T	N is value of the FILTER field; selections are 1-16. T is the period of the active timebase for that level.
Sequence level execution rate	30 ns	Time after sequential event occurs before next level is allowed.
RESET action	40 ns	Reset from sequential event to timer not guaranteed if sequential event has SYNC timebase. Reset from sequential event to counter only guaranteed if both seq. and global events use same filter clock.
Storage qualification	30 ns	WITH STORAGE field; selections are ON and OFF.
TO OCCUR nnnn TIMES	One count per valid event	Count of valid evts. before seq. evt. is satisfied; range is 1 - 9,999.
Delay (nnnn CLOCKS)	Delays up to 9,999 system clocks	Count of clocks before sequential event is satisfied.
EXT TRIG OUT		50 Ω source Z
Vout high (open) Vout high (50 Ω) Vout low (either)		3.8 V min. 1.9 V min. 0.6 V max., at 7 mA
Pulse width		70 ns min., 120 ns max.
Delay; probe tip clock to trigger out		65 ns min. 90 ns max.
EXT TRIG IN		
Input resistance Input capacitance V-input, max. Acceptance window		1 MΩ ± 1% 37 pF ± 5 pF ± 20 V Window length = 100 ns; window starts 50 ns after clock that causes trigger.

Table 8-5 (cont.)
1240 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
x1 Probes and 50 Ω terminated coax.		
Input threshold		1.4 V ± 100 mV
Minimum pulse ampl.		1.8 V high, 1.0 V low
Minimum pulse width		20 ns
x10 Probes		
Input threshold		1.4 V ± 500 mV
Minimum pulse ampl.		2.4 V high, 0.6 V low
Minimum pulse width		30 ns
Minimum slew rate		5 V/μs
Time between triggers for linked 1240s		Slave trigger within 60 ns of master trigger
T2 DEMUX CONTROL		
Phase Delay between first phase (T2 F) and last phase (T2 L)	10 ns min.	Only first occurrence of next phase is valid. Successive clocks without an intervening alternate phase are ignored.
Phase delay between last phase (T2 L) and first phase (T2 F)	20 ns min.	
ASYNC TIMEBASE		10 ns to 1 s in 1-2-5 increments (0.01% average accuracy)
TWO TIMEBASE CORRELATION		
Resolution of precedence between timebases.	10 ns	The 1240 can resolve the difference between a T1 and a T2 event if they occur 10 ns or more apart. If they occur < 10 ns from each other, the timebase that was previously indicated as occurring first will be indicated as occurring last.

Table 8-6
1240 ENVIRONMENTAL SPECIFICATIONS

Characteristic	Description
Temperature	
Maximum operating	+55°C
Minimum operating	−10°C
Non-operating	−62°C to +85°C
Humidity	95% to 97% relative humidity (Five 24 hr. cycles at 30°C to 60°C, instrument must reside in ≤ 70% relative humidity for two hours before and during operation)
Altitude	
Operating	4.5 km (15,000 ft.)
Non-operating	15 km (50,000 ft.)
Vibration, operating	
Displacement	0.025 inch (0.64 mm)
Frequency range	10 to 55 Hz
Shock	30 G's, halfsine, 11 ms duration, 18 shocks total, 3 on each face
Electromagnetic interference	Meets FCC part 15, sub-part J, class A, without probes. Meets VDE 0871, class B, without probes.

Table 8-7
1240 PHYSICAL SPECIFICATIONS

Characteristic	Description
Weight	12.0 kg (26.5 lbs.)
Overall Dimensions	
Height (handle folded back)	19.7 cm (7.8 inches)
Width (including handle)	36.8 cm (14.5 inches)
Length (including protective front cover)	49.8 cm (19.6 inches)

Table 8-8
1240D1 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
MEMORY CONFIGURATION		
Width		9 stored data channels; 1 non-stored clock/qualifier chan.
Depth		Glitches On / Glitches Off
no chaining		257 513
2 1240D1s chained		513 1025
3 1240D1s chained		769 1537
4 1240D1s chained		1025 2049
TIMEBASE GENERATION		
Clock Input		
Pulse Width	8 ns min.	
Period	20 ns min.	Min. time between OR'd clks is 25 ns
Amplitude	± 350 mV min. above and below programmed threshold	
Qualifier Input		
Setup time	11 ns max.	Values based on 1240D1 equipped with P6460 Data Acquisition Probe. Single selected qualifier driven.
Hold time	0 ns max.	
SYNCHRONOUS OPERATION		Uses signals specified by operator in Timebase menu. Can be used with all timebases.
Data, all channels		Data word width = 14 ns min. Setup and hold values based on 1240D1 equipped with P6460 Data Acquisition Probe.
Setup time	7 ns	4 ns setup time for single channel driven
Hold time	0.5 ns (T1 sourced from 1240D1)	2 ns hold time if data acquired on one type of acq. card and clk. source on other type.
Amplitude	± 350 mV min. above and below programmed threshold	

Table 8-8 (cont.)
1240D1 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
SYNC Events		
Global event for all channels		At max. SYNC rate, any input event meeting setup and hold times and min. word width.
Sequential event for all channels		At max. SYNC rate, recognize any input event meeting setup and hold times and min. word width. Up to 14 different events, one per sequence level.
ASYNCHRONOUS OPERATION		
Data min. word width guar. to be sampled	Timebase period + 6 ns	Timebase period + 8 ns with 1240D2; N samples of word requires (N×T)+6 ns min. word width ((N×T)+8 ns with 1240D2)
Glitch Capture		
Glitch width		6 ns at threshold (single chan.) at max. glitch/data transition rate of 30 ns Glitch may be detected as both glitch & data if transition occurs within 2 ns of sample clk.
Glitch amplitude	± 350 mV above and below programmed threshold	
ASYNC Events		N samples of word requires (N×T)+6 ns min. word width ((N×T)+8 ns with 1240D2)
Global event, all chans. min. data word width guar. to be sampled		
Clocked (1, 0, X, ◆)	Timebase period + 6 ns	Timebase period + 8 ns with 1240D2
Unclocked (1, 0, X)	16 ns min.	Min. width of valid event when global filter = 1 at 10NS and no 1240D2 channels specified
Sequential Event (1, 0, X)	Timebase period + 6 ns	Timebase period + 8 ns with 1240D2
PROBE THRESHOLD		
Threshold range		Selectable from +6.35 to −6.35 V in 50 mV increments; also includes preset values for TTL (+1.4 V), TPG (+3.70 V), −ECL (−1.30 V)
Accuracy	± 0.5% ± 65 mV	

Table 8-9
1240D2 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
MEMORY CONFIGURATION		
Width		18 stored data channels; 2 non-stored clock/qualifier chans.
Depth		
no chaining		513
2 1240D2s chained		1025
3 1240D2s chained		1537
4 1240D2s chained		2049

Table 8-9 (cont.)
1240D2 ELECTRICAL SPECIFICATIONS

Characteristic	Performance Requirements	Supplemental Information
TIMEBASE GENERATION		
Clock Input		
Pulse Width	8 ns min.	
Period	20 ns min.	Min. time between OR'd clocks is 25 ns
Amplitude	± 350 mV min. above and below programmed threshold	
Qualifier Input		Single, selected qualifier driven. Values based on 1240D2 equipped with P6460 Data Acq. Probes.
Setup time	11 ns max.	
Hold time	0 ns max.	
SYNCHRONOUS OPERATION		Uses signals specified by operator in Timebase menu. Can be used with all timebases. Setup and hold values based on a 1240D2 equipped with P6460 Data Acquisition Probes.
Data, all channels		
Setup time	12 ns	
Hold time	0 ns	
Amplitude	± 350 mV min. above and below programmed threshold	
SYNC Events		
Global event for all channels		At max. SYNC rate, any input event meeting setup and hold times.
Sequential event for all channels		At max. SYNC rate, recognize any input event meeting setup and hold times. Up to 14 different events, one per sequence level.
ASYNCHRONOUS OPERATION		
Data min. word width guaranteed to be sampled	Timebase period + 6 ns	Timebase period + 8 ns with 1240D1; N samples of word requires (N×T)+6 ns min. word width ((N×T)+8 ns with 1240D1)
ASYNC Events		N samples of word requires (N×T)+6 ns min. word width ((N×T)+8 ns with 1240D2)
Global evt., all chans. min. data word width guar. to be sampled		
Clocked (1, 0, X)	Timebase period + 6 ns	Data stored may be different than that recognized by event recognizer; Timebase period + 8 ns with 1240D1
Unclocked (1, 0, X)	16 ns min.	Minimum width of valid event when global filter = 1 at 10NS and no 1240D1 channels specified
Sequential Event (1, 0, X)	Timebase period + 6 ns	Timebase period + 8 ns with 1240D1
PROBE THRESHOLD		
Threshold range		Selectable from +6.35 to −6.35 V in 50 mV increments; also includes preset values for TTL (+1.4 V), TPG (+3.70 V), −ECL (−1.30 V)
Accuracy	± 0.5% ± 65 mV	

ERROR AND PROMPT MESSAGES

ALL AVAILABLE LEVELS ARE DEFINED: CHANGE AN EXISTING LEVEL	You tried to use the ADD LEVEL soft key when all 14 sequence levels are defined.
ALL AVAILABLE LOCATIONS DEFINED: CHANGE AN EXISTING LOCATION	You tried to add a new line to the search pattern when all eight lines (maximum) are already defined.
APPLYING SEARCH PATTERN — PLEASE WAIT	This message is displayed whenever the search pattern is applied to memory. The function can take several seconds to complete.
CANNOT EDIT AN EMPTY REFMEM	This message is displayed when you try to access the Reference Memory Editor menu when the current REFMEM contains no data.
	The following five error messages can occur whenever you display ACQMEM or REFMEM, use the COMPARE ACQMEM TO REFMEM Auto-Run condition, or press the LOAD FROM ACTIVE CURSOR soft key.
CONFIG ERROR: (ACQMEM/REFMEM) ABSENT MEMORIES ARE (list of pod numbers)	Memory to be displayed was downloaded from a ROM or RAM pack or from a remote controller, and was acquired on a 1240 with a different configuration than the current instrument setup. The pod numbers listed correspond to the unused memory segments in the downloaded memory. (Refer to *Memory Width vs. Depth* in Section 3 for a definition of memory segment.) The downloaded memory cannot be displayed unless the 1240's configuration is changed.
CONFIG ERROR: (ACQMEM/REFMEM) 9 CHANNEL CARDS ARE (width) BY (depth)	Memory to be displayed was stored with different 9-channel width vs. depth parameters than the current instrument setup.
CONFIG ERROR: (ACQMEM/REFMEM) 18 CHANNEL CARDS ARE (width) BY (depth)	Memory to be displayed was stored with different 18-channel width vs. depth parameters than the current instrument setup.
CONFIG ERROR: (ACQMEM/REFMEM) T1 MEMORIES ARE: (list of pod numbers)	Memory to be displayed was stored with different T1-pod assignments than the current instrument setup.
CONFIG ERROR: (ACQMEM/REFMEM) T2 MEMORIES ARE: (list of pod numbers)	Memory to be displayed was stored with different T2-pod assignments than the current instrument setup.
DIRECTORY FULL: DELETE AN EXISTING FILE FROM THE RAM PACK	This message is displayed when the area of the RAM pack reserved for storing file names is full, and you tried to store another file.

(cont.)

DON'T CARE INVALID IN THE REFMEM	Don't care (X) is not a valid character in the Reference Memory Editor menu.
GLITCH CAPTURE NOT ENABLED	You cannot enter a glitch symbol in the Trigger Spec or Search Pattern Entry menus when **GLITCHES OFF** is selected in the Memory Config menu. You cannot edit a glitch into reference memory if **GLTICHES OFF** was selected when the REFMEM data was acquired.
GLITCH INVALID IN A MASK FIELD	The glitch symbol is not a valid entry for the MASK fields in the COMPARE ACQMEM TO REFMEM Auto-Run condition.
GLITCH INVALID ON 18-CHANNEL CARD	You tried to enter the glitch symbol for a channel acquired by an 18-channel card. An 18-channel card cannot acquire glitches.
GLITCH INVALID WITH SYNCHRONOUS TIMEBASE	You tried to enter the glitch symbol for a group that is assigned a synchronous timebase.
GLITCH INVALID WITH UNCLOCKED GLOBAL EVENT RECOGNIZER	You tried to enter the glitch symbol in the global event recognizer when GLOBAL EVENT = **UNCLOCKED** is selected in the Timebase menu.
GROUP FULL: CANNOT INSERT CHANNEL	You touched INSERT CHANNEL for a group that already has the maximum of 36 channels.
HIGHLIGHTING OFF	You touched NEXT HIGHLIGHT DATA but the HIGHLIGHT field is set to **OFF**.
INVALID CHANNEL NUMBER	You tried to enter a value other than 0-8 or X in a CHAN field.
INVALID CHECKSUM: PACK IGNORED	The verification routine that runs when you press the LOAD NEW PACK soft key found a checksum error in the newly installed ROM pack.
INVALID CHECKSUM: "X" INITS PACK, ANY OTHER HARD KEY IGNORES IT	When you install a RAM pack and touch the LOAD NEW PACK soft key, this message is displayed if the pack verification routine detects a checksum error. Press X to clear and format the pack for use. This message is normal when a new, unused RAM pack is installed.
INVALID INPUT FOR BINARY RADIX INVALID INPUT FOR OCTAL RADIX	You tried to enter a digit too large for the selected radix. Valid binary values are 0 and 1; valid octal values are 0-7.
INVALID INPUT FOR PARTIAL DIGIT	You entered a number too large to fit in the number of bits remaining in the digit. For example: if a group is made up of 10 channels and the input radix is HEX, the input fields for this group will have three digits. The largest value you can enter is 3FF. If you try to enter 4-F for the high-order digit, this error message is displayed.

(cont.)

INVALID OPERATION: FILE TYPE NOT RECOGNIZED	You can store special file types (created by ROM packs) into a RAM pack. This message is displayed when you try to load a special file from a RAM pack and the 1240 no longer contains the internal parameters set up by the ROM pack to use the special file. Refer to the ROM pack manual for complete details.
INVALID OPERATION: FILES CANNOT BE DELETED FROM A ROM PACK	You tried to delete a file stored in a ROM pack. New files cannot be added to ROM packs, and existing files cannot be deleted.
INVALID OPERATION: NO FILES TO (DELETE/LOAD)	You touched LOAD FILE or DELETE FILE in the Storage Memory Manager menu when there were no files in the EXISTING FILES list.
INVALID POD NUMBER	The number you tried to enter in the POD field corresponds to a pod that either does not exist, is not assigned to the type of card you are building groups for, or has a different timebase than that already defined for the group.
INVALID SETUP: INCONSISTENT DATA OR HARDWARE REQUIREMENTS	Before a setup is loaded into the 1240 from a ROM or RAM pack, it is tested for certain conditions. This message is displayed when you press LOAD FILE and the setup does not pass the verification tests. This might happen if the setup is based on a different 1240 configuration or if the file is corrupt.
MEMORY FULL: DELETE AN EXISTING FILE FROM	You pressed the STORE NEW FILE soft key and there is not enough storage space remaining in the selected storage area.
MEMORIES CAN ONLY BE STORED INTO A RAM PACK	You pressed STORE NEW FILE in the Storage Memory Manager menu with a FILETYPE of ACQMEM or REFMEM, but the selection in the STORED IN field was not PACK.
MOVE FIELD CURSOR TO A CHANNEL SELECTION FIELD	You touched DISPLAY NEXT CHANNEL in the Timing Diagram when the field cursor was not in a channel selection (trace name) field.
MOVE FIELD CURSOR TO A GROUP DEFINITION FIELD	You pressed CLEAR GROUP with the field cursor positioned on the CARD TYPE field.
MOVE FIELD CURSOR TO A POD OR CHAN FIELD	You tried to use DELETE CHANNEL, ADD NEXT CHANNEL, or INSERT CHANNEL when the field cursor was not on a POD or CHAN field.
MOVE FIELD CURSOR TO A SEQUENCE LEVEL	You tried to delete a level of the sequential event recognizer when the field cursor was not positioned in a level.
MOVE FIELD CURSOR TO AN ASSIGNED CHANNEL	You touched the ADD NEXT CHANNEL soft key when the field cursor was positioned on an undefined channel (POD and/or CHAN value of X).

(cont.)

MOVE FIELD CURSOR TO AN EVENT RECOGNIZER GROUP FIELD	You touched LOAD FROM ACTIVE CURSOR in the Trigger Spec menu when the field cursor was not positioned in an event recognizer value field.
NO DATA TO EDIT IN CURRENT GROUPING	This message is displayed in the Reference Memory Editor menu when the 1240 has acquired data but has no grouping information for those channels and, therefore, cannot display the data.
NO GROUPS DEFINED: CANNOT EXIT MENU	You cannot exit the Channel Grouping menu if all groups are unspecified (all channels in the UNUSED list).
NO HIGHLIGHTED LOCATIONS OCCUR	You touched NEXT HIGHLIGHT DATA and no data meeting the highlight requirements was found.
NO SUCCESSOR TO CHANNEL 0	You tried to add another channel to a group with the ADD NEXT CHANNEL soft key when the field cursor was positioned on a CHAN value of 0.
NO VALID DATA ACQUIRED	This error message can be displayed for either of the following two reasons: 1. No data was acquired; acquisition memory is empty. This can occur if the sampling clock is SYNC and no clocks occur. It can also occur if you use clock and/or storage qualification to reject all clocks and/or data. 2. The current clock setup violates the 1240's clock specifications. (Data is acquired, but it is not valid.) For example: The clock specifications are violated if you try to clock the 1240 faster than 20 ns SYNC. The clock specifications can also be violated if you change the card threshold during the COMPARE ACQMEM TO REFEMEM Auto-Run mode, and the clock line is noisy.
OPERATION IN PROGRESS — PLEASE WAIT	This message is displayed when you store or load a memory file in the Storage Memory Manager menu. Storing and loading operations can take several seconds to complete.
PATTERN SEARCH DISABLED	You selected pattern highlighting in the State Table or Timing Diagram but the PATTERN SEARCH **DISABLED** selection is currently in effect in the Search Pattern Entry menu.
PRESS "STOP" TO TERMINATE ACQUISITION	The five MENU keys and STOP are the only valid key inputs while the 1240 is acquiring data. When you press one of the MENU keys, acquisition stops, and the 1240 displays the last menu accessed in that menu group. When you press STOP, acquisition stops, and the 1240 displays data in state table or timing diagram format. During COMPARE ACQMEM TO REFMEM status display operations, only STOP is valid.

(cont.)

PRESS "X" TO CONFIRM OPERATION (ANY OTHER HARD KEY CANCELS IT)	This is not an error message. It is displayed when you touch a soft key that requires verification before the action is taken.
SELECTED FILETYPE CAN ONLY BE STORED INTO A RAM PACK	The file to be stored is an ACQMEM, REFMEM, or special file type (from a previously-installed ROM pack) but the selected storage area is not **PACK**. Nonvolatile memory and internal RAM can store only instrument setups; memories and other special file types can only be stored in a RAM pack.
UNKNOWN PACK TYPE: PACK IGNORED	The verification routine that runs when you touch the LOAD NEW PACK soft key did not recognize the newly installed ROM pack as a valid 1240 pack. This occurs when the ROM pack is not a 1240 pack, or if it is defective.
UNKNOWN RAM PACK: "X" INITS PACK, ANY OTHER HARD KEY IGNORES IT	When you install a RAM pack and touch the LOAD NEW PACK soft key, this message is displayed if the pack verification routine cannot identify the pack. Press the X key on the front panel to clear and format the pack for use. This message is normal when a new, unused RAM pack is installed.
USE 0-9	You tried to enter a non-decimal value into a decimal field.
USE 0 OR 1	You tried to enter a number other than 0 or 1 in a POLARITY field.
USE 1-E	You tried to enter something besides 1-E in the TO LEVEL field (displayed when JUMP IF/JUMP IF NOT is selected in the sequential event recognizer).
USE SELECT KEYS	You tried to use the data entry keys to enter a value into a field controlled by the SELECT keys.
WARNING: 10 NS INVALID - GLITCH ENABLED and/or 18 CHANNEL CARD USES T1	The 10 NS selection for T1 ASYNC is not available because glitch storage is enabled in the Memory Config menu, and/or an 18-channel card is assigned to T1. For 10 ns acquisition, glitch storage must be disabled, and all 18-channel cards must be assigned T2. Refer to *10 ns Acquisition* in Section 3 for more information.
WARNING: JUMP TO UNDEFINED LEVEL CAUSES TRIGGER	You entered the number of a level not currently defined in the sequential event recognizer into the TO LEVEL field (displayed when JUMP IF/-JUMP IF NOT is selected).
WARNING: MAXIMUM VALUE USED	This message is displayed if you try to enter too large a numeric value into certain fields. The 1240 sets the field to its maximum value.

(cont.)

WARNING: MINIMUM VALUE USED	You tried to enter a numeric value lower than the acceptable minimum for a field. The 1240 sets the field to its minimum value.
WARNING: SETUP INFORMATION IN OTHER MENUS WILL BE LOST	This message is displayed when you change the Operation Level to a lower number and the existing setup was specified under a higher number. Refer to Table 8-1 for a description of the possible changes.
WARNING: T1 STORAGE QUALIFICATION DISABLED AT 10 NS	This message is displayed in the Trigger Spec menu when T1 is ASYNC 10 NS, and you select STORE in the global event recognizer. The 1240 does not support storage qualification for T1 channels at 10 ns. At 10 ns, all T1 data is stored.

DIFFERENCES BETWEEN OPERATION LEVELS

Table 8-10
DIFFERENCES BETWEEN THE OPERATION LEVELS

Level	Timebase Menu	Memory Config Menu	Trigger Spec Menu
0	Only T1 CLOCKED/UNCLOCKED not displayed	No Chaining	LOOK FOR TRIGGER and FILTER fields not displayed. WITH STORAGE fields not displayed in sequential event recognizer.
1	Only T1	Full Operation	WITH STORAGE fields not displayed in sequential event recognizer.
2	T1 , T2 CLOCKED/UNCLOCKED not displayed	Full Operation	FILTER fields not displayed.
3	Full Operation	Full Operation	Full Operation

TEST PATTERN GENERATOR INFORMATION

The test pattern generator (TPG) simulates a data source by sending a data pattern of 63 unique values to the two sets of pins located directly above the probe connections on the right side panel of the 1240. A different pattern is available from both TPG outputs; these patterns are listed below in Tables 8-11 and 8-12.

The TPG MODE field in the Operation Level menu (see Section 3) lets you select how the patterns will be clocked and whether the patterns will contain glitches. Table 8-13 describes the characteristics of the different TPG modes. Mode 0 is the power-up default. Figures 8-1 and 8-2 explain the clock and data outputs for the different modes.

When you acquire data from the TPG, you must set the THRESHOLD fields for the cards connected to the TPG outputs to **TPG**. This selection sets the card input threshold to +3.70 V, to correspond to the TPG output levels.

NOTE

The TPG can only be used with the P6460 Data Acquisition Probe.

The TPG is only guaranteed to operate properly within the temperature range +20° C to +30° C.

Table 8-11
TPG PATTERN FROM LEFT CONNECTOR

1FF	1AE	071	186
1BE	15D	0A2	10C
17D	0FB	145	018
0BA	1B6	0CB	030
175	16D	1D7	061
0AA	09A	1EF	082
155	134	19E	104
0EB	069	13C	008
196	092	079	010
12C	124	0B2	020
059	049	165	041
0F3	0D3	08A	0C3
1A6	1E7	114	1C7
14D	18E	028	1CF
0DB	11C	051	1DF
1F7	038	0E3	

Table 8-12
TPG PATTERN FROM RIGHT CONNECTOR

1FF	175	18E	030
1F7	0EB	114	061
1EF	1DF	028	0C3
1D7	1B6	059	186
1AE	16D	0BA	10C
155	0D3	17D	010
0AA	1A6	0F3	020
15D	14D	1E7	041
0B2	092	1CF	082
165	124	196	104
0CB	049	12C	008
19E	09A	051	018
134	13C	0A2	038
069	071	145	079
0DB	0E3	08A	0FB
1BE	1C7	11C	

Table 8-13
TPG MODES

Mode	With Glitches	Clocked At
0	No	12 MHz
1	Yes	6 MHz
2	No	T1
3	Yes	T1 ÷ 2

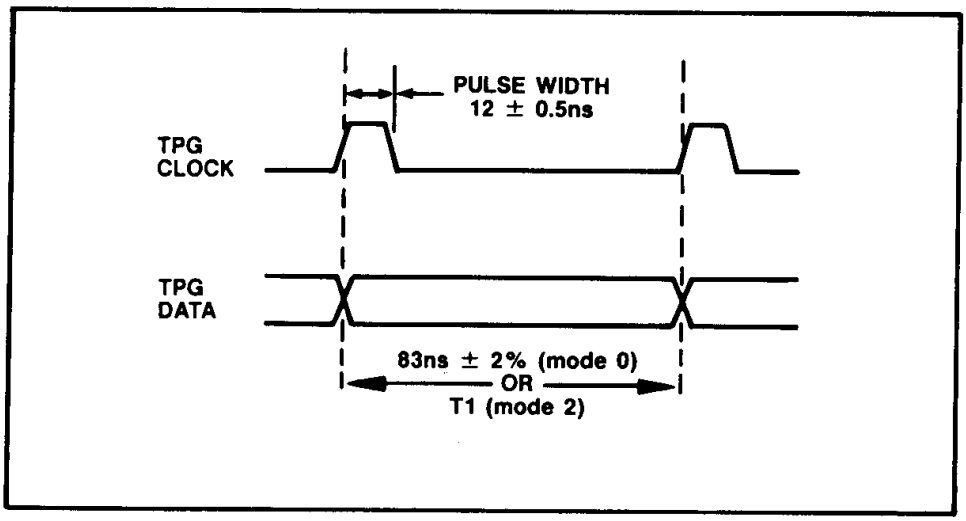

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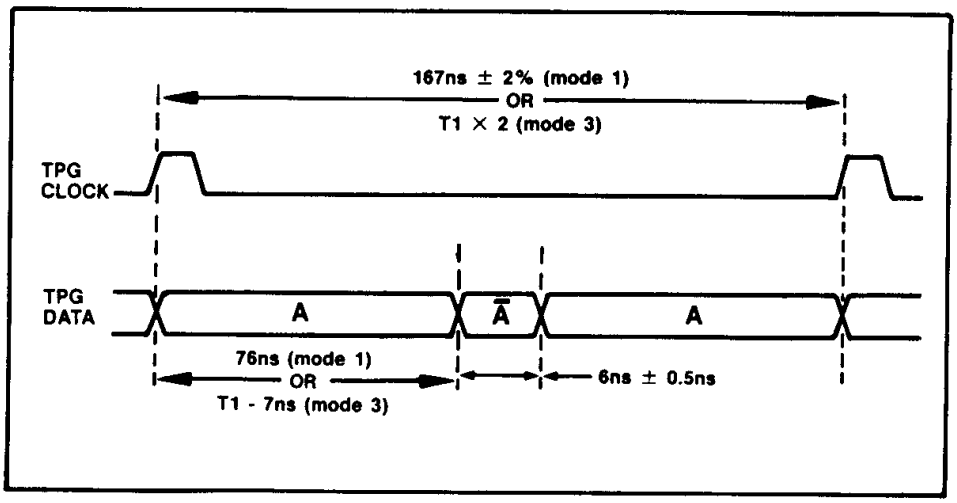
Figure 8-1. Mode 0 and mode 2 TPG outputs. In mode 0, the clock is derived from a 12 MHz oscillator which is internal to the TPG. In mode 2, the clock source is timebase T1 (specified in the Timebase menu); the TPG output is only valid when T1 is less than or equal to 50 MHz.



4340–52

Figure 8-2. Mode 1 and mode 3 TPG outputs. In mode 1, the clock is derived from a 12 MHz oscillator which is internal to the TPG. Alternate clock cycles are used to produce glitches, so the actual frequency of the output is 6 MHz. In mode 3, the clock source is timebase T1 (specified in the timebase menu) and the output period is T1 x 2. The TPG output is only valid when T1 is less than or equal to 50 MHz.

OCTAL-HEX-ASCII CONVERSION CHART

OCT	HEX	ASC	OCT	HEX	ASC	OCT	HEX	ASC	OCT	HEX	ASC
000	00	NUL	040	20	SP	100	40	@	140	60	`
001	01	SOH	041	21	!	101	41	A	141	61	a
002	02	STX	042	22	"	102	42	B	142	62	b
003	03	ETX	043	23	#	103	43	C	143	63	c
004	04	EOT	044	24	$	104	44	D	144	64	d
005	05	ENQ	045	25	%	105	45	E	145	65	e
006	06	ACK	046	26	&	106	46	F	146	66	f
007	07	BEL	047	27	'	107	47	G	147	67	g
010	08	BS	050	28	(	110	48	H	150	68	h
011	09	HT	051	29	)	111	49	I	151	69	i
012	0A	LF	052	2A	*	112	4A	J	152	6A	j
013	0B	VT	053	2B	+	113	4B	K	153	6B	k
014	0C	FF	054	2C	,	114	4C	L	154	6C	l
015	0D	CR	055	2D	–	115	4D	M	155	6D	m
016	0E	SO	056	2E	.	116	4E	N	156	6E	n
017	0F	SI	057	2F	/	117	4F	O	157	6F	o
020	10	DLE	060	30	0	120	50	P	160	70	p
021	11	DC1	061	31	1	121	51	Q	161	71	q
022	12	DC2	062	32	2	122	52	R	162	72	r
023	13	DC3	063	33	3	123	53	S	163	73	s
024	14	DC4	064	34	4	124	54	T	164	74	t
025	15	NAK	065	35	5	125	55	U	165	75	u
026	16	SYN	066	36	6	126	56	V	166	76	v
027	17	ETB	067	37	7	127	57	W	167	77	w
030	18	CAN	070	38	8	130	58	X	170	78	x
031	19	EM	071	39	9	131	59	Y	171	79	y
032	1A	SUB	072	3A	:	132	5A	Z	172	7A	z
033	1B	ESC	073	3B	;	133	5B	[	173	7B	{
034	1C	FS	074	3C	<	134	5C	\	174	7C	¦
035	1D	GS	075	3D	=	135	5D	]	175	7D	}
036	1E	RS	076	3E	>	136	5E	^	176	7E	~
037	1F	US	077	3F	?	137	5F	_	177	7F	DEL

OCTAL–HEX–EBCDIC CONVERSION CHART

OCT	HEX	EBC	OCT	HEX	EBC	OCT	HEX	EBC	OCT	HEX	EBC
000	00	NUL	100	40	SP	200	80		300	C0	{
001	01	SOH	101	41		201	81	a	301	C1	A
002	02	STX	102	42		202	82	b	302	C2	B
003	03	ETX	103	43		203	83	c	303	C3	C
004	04	PF	104	44		204	84	d	304	C4	D
005	05	HT	105	45		205	85	e	305	C5	E
006	06	LC	106	46		206	86	f	306	C6	F
007	07	DEL	107	47		207	87	g	307	C7	G
010	08	GE	110	48		210	88	h	310	C8	H
011	09	RLF	111	49		211	89	i	311	C9	I
012	0A	SMM	112	4A	¢	212	8A		312	CA	
013	0B	VT	113	4B	.	213	8B		313	CB	
014	0C	FF	114	4C	<	214	8C		314	CC	
015	0D	CR	115	4D	(	215	8D		315	CD	
016	0E	SO	116	4E	+	216	8E		316	CE	
017	0F	SI	117	4F	|	217	8F		317	CF	
020	10	DLE	120	50	&	220	90		320	D0	}
021	11	DC1	121	51		221	91	j	321	D1	J
022	12	DC2	122	52		222	92	k	322	D2	K
023	13	TM	123	53		223	93	l	323	D3	L
024	14	RES	124	54		224	94	m	324	D4	M
025	15	NL	125	55		225	95	n	325	D5	N
026	16	BS	126	56		226	96	o	326	D6	O
027	17	IL	127	57		227	97	p	327	D7	P
030	18	CAN	130	58		230	98	q	330	D8	Q
031	19	EM	131	59		231	99	r	331	D9	R
032	1A	CC	132	5A	!	232	9A		332	DA	
033	1B	CU1	133	5B	$	233	9B		333	DB	
034	1C	IFS	134	5C	*	234	9C		334	DC	
035	1D	IGS	135	5D	)	235	9D		335	DD	
036	1E	IRS	136	5E	;	236	9E		336	DE	
037	1F	IUS	137	5F	¬	237	9F		337	DF	
040	20	DS	140	60	-	240	A0		340	E0	\
041	21	SOS	141	61	/	241	A1	~	341	E1	
042	22	FS	142	62		242	A2	s	342	E2	S
043	23		143	63		243	A3	t	343	E3	T
044	24	BYP	144	64		244	A4	u	344	E4	U
045	25	LF	145	65		245	A5	v	345	E5	V
046	26	ETB	146	66		246	A6	w	346	E6	W
047	27	ESC	147	67		247	A7	x	347	E7	X
050	28		150	68		250	A8	y	350	E8	Y
051	29		151	69		251	A9	z	351	E9	Z
052	2A	SM	152	6A	¦	252	AA		352	EA	
053	2B	CU2	153	6B	,	253	AB		353	EB	
054	2C		154	6C	%	254	AC		354	EC	
055	2D	ENQ	155	6D	_	255	AD		355	ED	
056	2E	ACK	156	6E	>	256	AE		356	EE	
057	2F	BEL	157	6F	?	257	AF		357	EF	
060	30		160	70		260	B0		360	F0	0
061	31		161	71		261	B1		361	F1	1
062	32	SYN	162	72		262	B2		362	F2	2
063	33		163	73		263	B3		363	F3	3
064	34	PN	164	74		264	B4		364	F4	4
065	35	RS	165	75		265	B5		365	F5	5
066	36	UC	166	76		266	B6		366	F6	6
067	37	EOT	167	77		267	B7		367	F7	7
070	38		170	78		270	B8		370	F8	8
071	39		171	79	`	271	B9		371	F9	9
072	3A		172	7A	:	272	BA		372	FA	|
073	3B	CU3	173	7B	#	273	BB		373	FB	
074	3C	DC4	174	7C	@	274	BC		374	FC	
075	3D	NAK	175	7D	'	275	BD		375	FD	
076	3E		176	7E	=	276	BE		376	FE	
077	3F	SUB	177	7F	"	277	BF		377	FF	EO

OPTIONS AND ACCESSORIES

Options

Option A1, Universal Euro Plug, 250V/6A
Option A2, United Kingdom Plug, 240V/6A
Option A3, Australian Plug, 250V/6A
Option A4, North American Plug, 240V/10A
Option A5, Switzerland Plug, 240V/6A

Standard Accessories

1 Accessory Pouch, 016-0707-00
1 Operator's Manual, 070-4340-00
5 Reference Guides, 070-4641-00
1240 Seminar Workbook, 062-6926-00
1 Power Cord, 161-0104-00
1 Front Panel Cover, 200-2780-00
2 Diagnostic Lead Sets, 012-0556-00

Optional Accessories

Acquisition Cards:
1240D1, 9-channel Acquisition Card
1240D2, 18-channel Acquisition Card

Data Acquisition Probes:
P6460 Data Acquisition Probe
P6462 Fixed Threshold TTL Acquisition Probe

Scope Probes:
P6120 x1 Scope Probe, 010-6120-00
P6105 x10 Encoded Scope Probe, 010-6105-00

COMMunication Packs:
1200C01, RS232C COMM Pack
1200C02, GPIB COMM Pack
1200C11, Parallel Printer COMM Pack

Memory Packs:
12RS01, Nonvolatile 8K RAM Pack
12RS11, 32K EPROM Pack (empty)
12RS12, 32K EPROM Pack (blank)

Documentation:
Empty half-size binder for optional accessory documentation, 062-6927-00

Service Accessories:
Service Maintenance Kit, 067-1103-01
includes: 12RD01, 1240 Diagnostic ROM Pack
Service Manual
Extender Card
Diagnostic Lead Set
Service Manual, 062-7124-00
12RD01, 1240 Diagnostic ROM Pack
Diagnostic Lead Set, 012-0556-00
1240 Extender Card, 670-7539-01

ROM Packs:
12R01, Performance Analysis ROM Pack
12RC01, Printer Support ROM Pack
12RC02, Master/Slave Support ROM Pack
12RM01, 8080 Mnemonics ROM Pack
12RM02, 8085 Mnemonics ROM Pack
12RM03, 8086 Mnemonics ROM Pack
12RM04, 8088 Mnemonics ROM Pack
12RM05, 80186 Mnemonics ROM Pack
12RM06, 80188 Mnemonics ROM Pack
12RM21, 6800 Mnemonics ROM Pack
12RM22, 6802 Mnemonics ROM Pack
12RM23, 6808 Mnemonics ROM Pack
12RM24, 6809 Mnemonics ROM Pack
12RM25, 68000 Mnemonics ROM Pack
12RM26, 68008 Mnemonics ROM Pack
12RM41, Z80 Mnemonics ROM Pack
12RM42, Z8001/3 Mnemonics ROM Pack
12RM43, Z8002/4 Mnemonics ROM Pack
12RM62A, F9450 (1750A MIL STD) Mnemonics ROM Pack
12RM63, 6502 Mnemonics ROM Pack
12RM71, NSC800 Mnemonics ROM Pack