

2304-BIT BIPOLAR RAM (256 × 9)

82S212 (T.S.)

DESCRIPTION

The organization of the 82S212 allows byte wide storage of data, including parity. Where parity is not required, the ninth bit can be used as a tag for each word stored. The 82S212 is ideal for scratch-pad, push-down stacks, buffer memories, and other internal memory applications in which space and performance requirements dictate a wide data path in favor of word depth.

The 82S212 data inputs and outputs are common (common I/O) with separate output disable (OD) line that allows ease of read/write operations using a common bus.

The 82S212 is available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to 75°C) specify N82S212F or N and for the military temperature range (-55°C to +125°C) specify S82S212F.

FEATURES

- **Address access time:**
N82S212: 45ns max
S82S212: 70ns max
- **Power dissipation: 0.3mW/bit**
- **Tri-state outputs**
- **Schottky clamped TTL**

APPLICATIONS

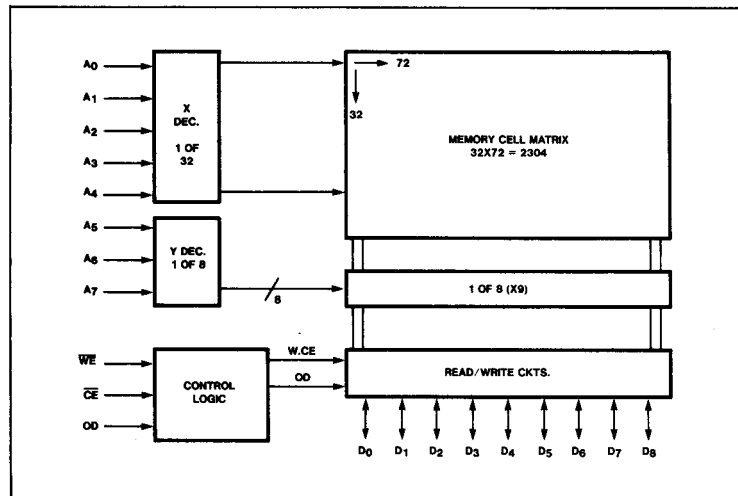
- **Cache memory**
- **Buffer storage**
- **Writable control store**

TRUTH TABLE

MODE	\overline{WE}	\overline{CE}	OD	D_N IN/OUT
Disable output	X	X	1	High Z
Disable R/W	X	1	X	High Z
Write	0	0	1	Data in
Read	1	0	0	Data out

X = Don't care

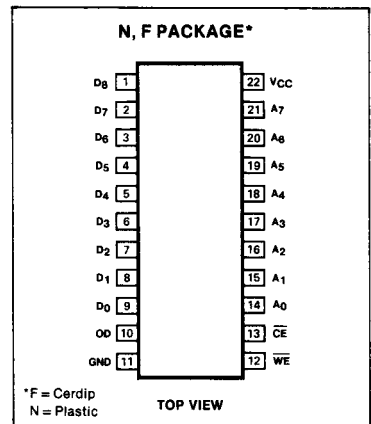
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

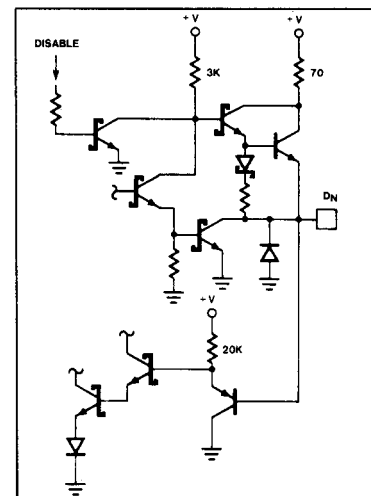
PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7
V_{IN}	Input voltage	+5.5
V_{O}	Off-state output voltage	+5.5
T_A	Temperature range	
	Operating	0 to +75
T_{STG}	Commercial	-55 to +125
	Military	-65 to +150
	Storage	

PIN CONFIGURATION



*F = Cerdip
N = Plastic

TYPICAL I/O STRUCTURE



2304-BIT BIPOLAR RAM (256 × 9)

82S212 (T.S.)

DC ELECTRICAL CHARACTERISTICS¹

N82S212: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S212: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER ¹	TEST CONDITIONS	N82S212			S82S212			UNIT			
		Min	Typ	Max	Min	Typ	Max				
V _{IL} V _{IH} V _{IC}	Input voltage Low High Clamp ²	V _{CC} = Min V _{CC} = Max V _{CC} = Min, I _{IN} = -12mA			2.0		.85 -1.5	2.2		.80 -1.5	V
V _{OL}	Output voltage Low ³	V _{CC} = Min, I _{OL} = 8.0mA					0.5			0.5	V
I _{IL} I _{IH}	Input current Low High	V _{IN} = 0.45V V _{IN} = 5.5V					-100 25			-150 40	μA
I _{O(OFF)} I _{OS}	Output current Hi-Z state Short circuit ^{4, 5}	CE = High or OD = High, V _{OUT} = 5.5V CE = High or OD = High, V _{OUT} = 0.5V CE = OD = Low, V _{OUT} = 0V			-20		40 -100 -70	-15		60 -100 -80	μA mA
I _{CC}	V _{CC} supply current ⁵	V _{CC} = Max				135	185			200	mA
C _{IN} C _{OUT}	Capacitance Input Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V				5 8			5 8		pF

AC ELECTRICAL CHARACTERISTICS¹

R₁ = 470Ω, R₂ = 1kΩ, C_L = 30pF
 N82S212: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V
 S82S212: -55°C ≤ T_A ≤ +125°C, 4.75V ≤ V_{CC} ≤ 5.25V

PARAMETER	TO	FROM	N82S212			S82S212			UNIT	
			Min	Typ ³	Max	Min	Typ ³	Max		
T _{AA}	Access time Address	Output	Address			45			70	ns
T _{OE} T _{CE}	Enable time Output Output	Output Output	OD Chip enable	5		25 25			50 50	ns
T _{OD} T _{CD}	Disable time Output Output	Output Output	OD Chip enable			25 25			50 50	ns
T _{WP}	Pulse width Write			25			45			ns
T _{WSC} T _{WHD}	Setup time Hold time	Write Chip enable	Chip enable Write	5 5			10 10			
T _{WSD} T _{WHD}	Setup time Hold time	Write Data	Data Write	25 5			45 5			
T _{WSA} T _{WHA}	Setup time Hold time	Write Address	Address Write	5 5			10 15			
T _{SO} T _{HO}	Setup time (from disabled state) Hold time	Chip enable OD	OD Chip enable	5 5			5 5			

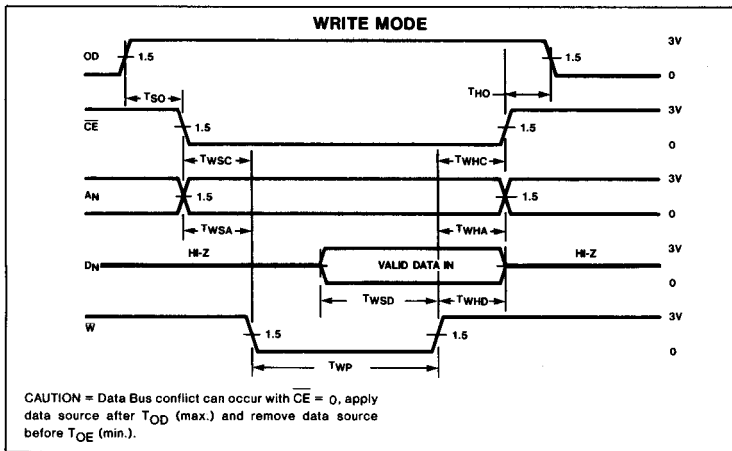
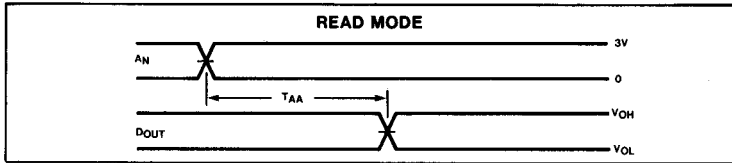
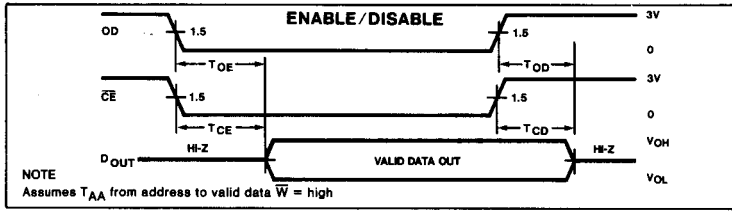
NOTES

- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2 minute warmup.
- All voltages are with respect to network ground terminal.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- Measured on one pin at a time.
- Duration of I_{OS} test should not exceed one second.

2304-BIT BIPOLAR RAM (256 × 9)

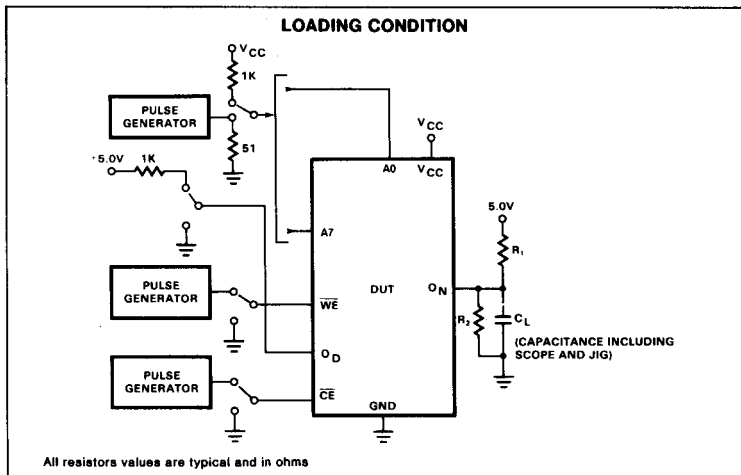
82S212 (T.S.)

TIMING DIAGRAMS



5

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

